27.1 A 250kHz-BW 93dB-SNDR 4th-Order Noise-Shaping SAR Using Capacitor Stacking and Dynamic Buffering

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The noise-shaping (NS) SAR is an emerging hybrid architecture that aims to combine the benefits of both SAR and ΔΣ ADCs [1-8]. The key in an NS SAR is the NS filter. As shown in Fig. 27.1.1, prior NS filter techniques can be classified into two types. The first way is to use a closed-loop amplifier-based integrator [1-3]. With sufficient gain of the amplifier, this type of integrator can realize a sharp noise transfer function (NTF). However, the high-gain multi-stage amplifier produces large noise, is power-consuming and unfriendly to technology scaling [2,3]. The second way is to use passive charge sharing to perform error feedback [4-6] or integration [7,8]. The fully passive filter avoids using closed-loop amplifiers, but it has signal attenuation issue and the resulting NTF is mild [4]. Also, due to the lack of effective gain, it suffers from large comparator noise. To improve the NTF and noise suppression capability, some works place an open-loop amplifier before the passive filter [5-7], or implement a passive gain after it [8]. However, the gain of an open-loop amplifier is sensitive to PVT variations, and the passive gain method suffers from severe parasitic effects when a large gain is required.

This paper presents an efficient way to implement a high-order and robust NS filter. It realizes an integrator by stacking the residue capacitor with the integration capacitor, and storing the stacking result through a unity-gain buffer. A source follower can be used as the buffer, which is simple and PVT robust. This NS filter does not rely on any amplifier, and realizes a sharp NTF with zeros close to the unit circle. It has low hardware complexity, and is easy to extend to high order. A 4th-order NS SAR is implemented in this work. It achieves 93.3dB SNDR over 250kHz bandwidth at the OSR of 10 while consuming 340μW power, leading to a Schreier FoM of 182dB.

To illustrate the operation principle, the 1st-order examples of the proposed NS technique are shown in Fig. 27.1.1. First, the single-ended form is discussed. In an odd ADC operation cycle 2k-1, the integration capacitor C_o is stacked with the residue capacitor C_{res}, obtaining the sum of the residue voltage $V_{res}(2k-1)$ and the previous integration voltage $V_{int}(2k-2)$. The sum is the ideal integration result, but it cannot be directly used in consequent ADC conversions. To address this issue, another integration capacitor C_e is used to store the integration result $V_{int}(2k-1) = V_{res}(2k-1) + V_{int}(2k-2)$ through a unity-gain buffer. A ping-pong operation is performed between C_o and C_e. In the next even cycle 2k, C_e is stacked with C_{res} while C_o is used to store the new integration result $V_{int}(2k) = V_{res}(2k) + V_{int}(2k-1)$. In this way, the ideal integration is realized without using a closed-loop amplifier. A problem with the single-ended integration is that it is prone to saturation due to the DC component across the integration capacitor, which includes the buffer offset and the common-mode voltage mismatch at both ends of the capacitor. This problem can be solved by performing differential integration (placing the integration capacitor between the outputs of a differential buffer), and chopping the buffer and integration capacitors. Chopping also addresses the flicker noise of the buffer. In addition, for the same kT/C noise budget, the total integration capacitor size in a differential ADC can be 4× reduced by using differential integration, comparing with that using single-ended integration.

The proposed 4th-order NS SAR ADC is shown in Fig. 27.1.2 (the comparator and SAR logic are not shown for simplicity). Four groups of capacitors and differential buffers (C_{oi}–BF_i–C_{ei}, i=1~4) form a 4th-order integration network. During an odd operation cycle 2k-1, C_{o1} and C_{o4} are connected in series and stacked over the 9b DAC at the p-side (DAC_p, 16pF), while C_{o2} and C_{o3} are stacked over DAC_n. Since $C_{o1\sim4}$ hold the previous integration results $V_{int1\sim4}(2k-2)$, the stacking operation realizes the addition of the present input signal with $V_{int1\sim4}(2k-2)$. Therefore, a standard 1-input-pair comparator connected between the right sides of C_{o4} and C_{o3} can be used for the SAR conversion. At the end of SAR conversion, the residue voltage $V_{res}(2k-1)$ is obtained across the top plates of the DACs, and the buffers are enabled. BF_1 (connected across C_{o1}–DAC_p–DAC_n) delivers the 1st-order integration result $V_{int1}(2k-1) = V_{res}(2k-1) + V_{int1}(2k-2)$ to C_{e1}, BF_2 (connected across C_{o1}–DAC_p–DAC_n–C_{o2}) delivers the 2nd-order integration result $V_{int2}(2k-1) = V_{res}(2k-1) + V_{int1}(2k-2) + V_{int2}(2k-2)$ to C_{e2}, BF_3 (connected across C_{o1}–DAC_p–DAC_n–C_{o2}–C_{o3}) delivers the 3rd-order integration result $V_{int3}(2k-1) = V_{res}(2k-1) + V_{int1}(2k-2) + V_{int2}(2k-2) + V_{int3}(2k-2)$ to C_{e3}, and BF_4 (connected across C_{o4}–C_{o1}–DAC_p–DAC_n–C_{o2}–C_{o3}) delivers the 4th-order integration result $V_{int4}(2k-1) = V_{res}(2k-1) + V_{int1}(2k-2) + V_{int2}(2k-2) + V_{int3}(2k-2) + V_{int4}(2k-2)$ to C_{e4}. After integrations, the buffers are disabled to save power. During the next even cycle 2k, $C_{e1\sim4}$ are stacked over the DACs, and $C_{o1\sim4}$ are used to store the new integration results $V_{int1\sim4}(2k)$. Also, the integration network ($C_{e1\sim4}$–$BF_{1\sim4}$–$C_{o1\sim4}$) is flipped to perform chopping.

The differential buffer consists of a pair of flipped voltage followers (FVFs), as shown in Fig. 27.1.3. The FVFs are dynamically controlled by Φ_{en}. They are only powered during the integration phase (25% of an entire ADC operation cycle). Compared with a conventional source follower, the FVF provides smaller output resistance and therefore faster settling, but this is at the cost of larger noise. To reduce noise, the 2-phase settling technique is used [6]. A switch-controlled resistor R_a is added at the FVF output to adjust its bandwidth. During the first 15ns of the integration phase, R_a is bypassed to enable fast settling. During the remaining 35ns of the integration phase, R_a is switched in to limit the noise bandwidth. In this way, the proposed buffer combines the benefits of fast settling and low noise. The 2-phase settling is only used in BF_1, because the noise introduced by $BF_{2\sim4}$ can be shaped and thus is negligible. The integration capacitors and bias currents for $BF_{1/2/3/4}$ are $C_{1/2/3/4}$=8/8/2/2pF, $I_{b1/2/3/4}$=150/60/15/15μA, respectively. Monte Carlo simulation shows that the gain of the FVF is around 0.95 with 1% 3σ variation, which ensures a sharp and robust NTF.

Fabricated in 40nm CMOS, the prototype occupies 0.094mm² (Fig. 27.1.7) and consumes 340μW of power when operating under a 1.1V supply and a 5MS/s sampling rate. The DAC mismatch is addressed by a foreground calibration. Figure 27.1.4 shows the measured output spectrum with a 49kHz -1.2dBFS input. The SNDR, SNR and SFDR over a 250kHz bandwidth are 93.3dB, 94dB and 104.4dB, respectively. Figure 27.1.5 shows the measured SNDR/SNR versus input amplitude. The dynamic range (DR) is 95dB. To prove the robustness of the proposed NS technique, the measured SNDRs of 7 chips versus FVF supply are also given in Fig. 27.1.5. It shows that the SNDR variation is within 1dB across the 7 chips, and is within 0.3dB against ±10% supply changes.

Figure 27.1.6 compares this work with prior publications. By using capacitor stacking and buffering for integration, the proposed NS SAR avoids the signal attenuation of passive charge sharing. Also, it does not require a closed-loop or open-loop amplifier; the former is complex and power-consuming while the latter suffers from gain variation and leads to NTF variation. The simple source followers are used as the buffers in this work. Due to the stable unity gain of source followers, the proposed NS SAR realizes a robust and sharp NTF. The architecture is compact and easy to extend to high order. This work is the first NS SAR ADC that achieves >90dB SNDR with >100kHz bandwidth.

Acknowledgement:
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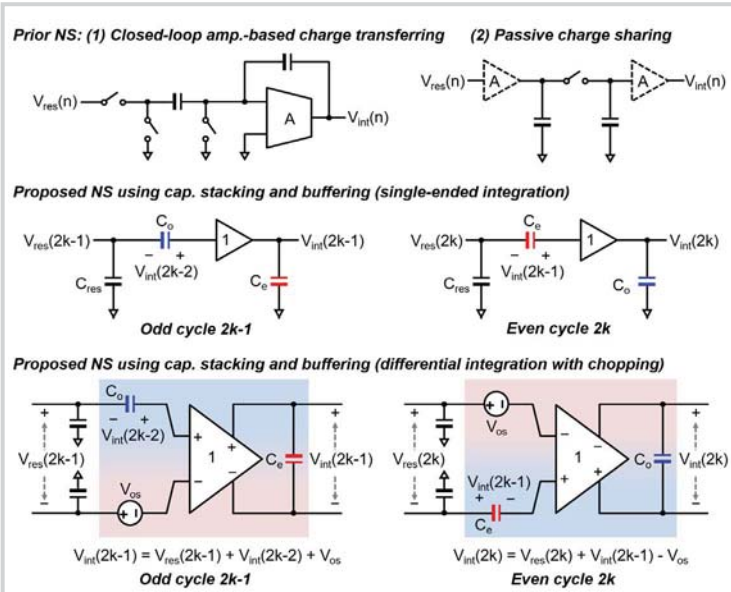

Figure 27.1.1: Principle of prior and proposed NS techniques (1st-order examples).

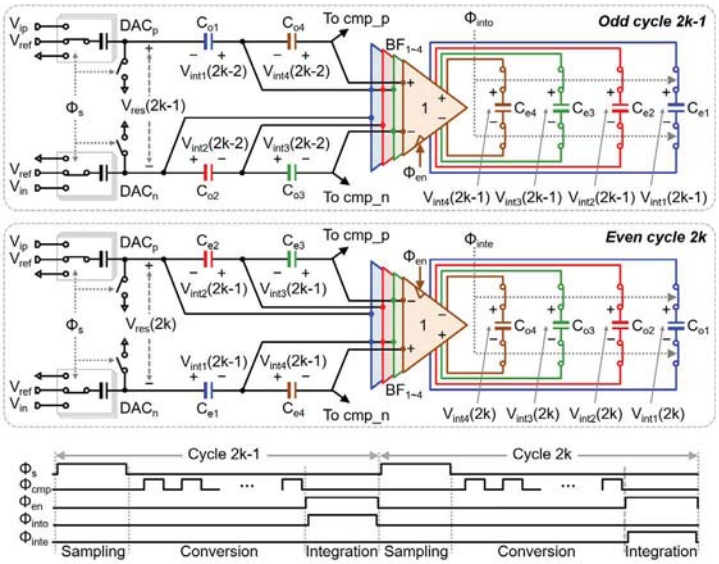

Figure 27.1.2: Proposed 4th-order NS SAR ADC.

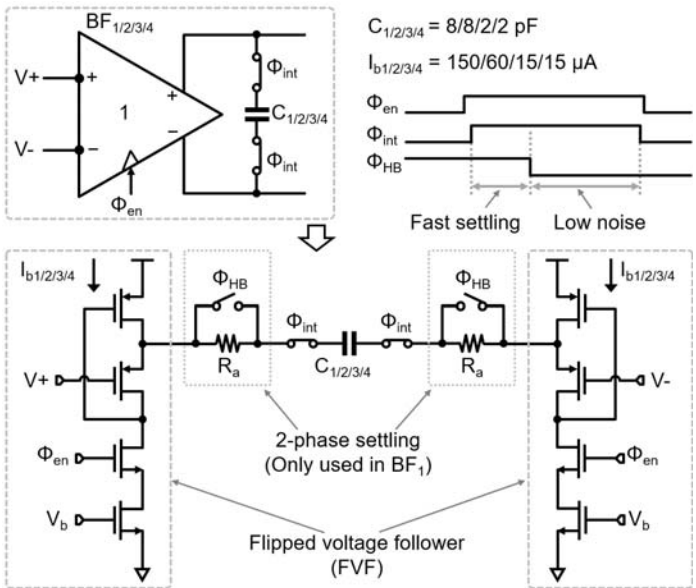

Figure 27.1.3: Circuit implementation of the differential buffer.

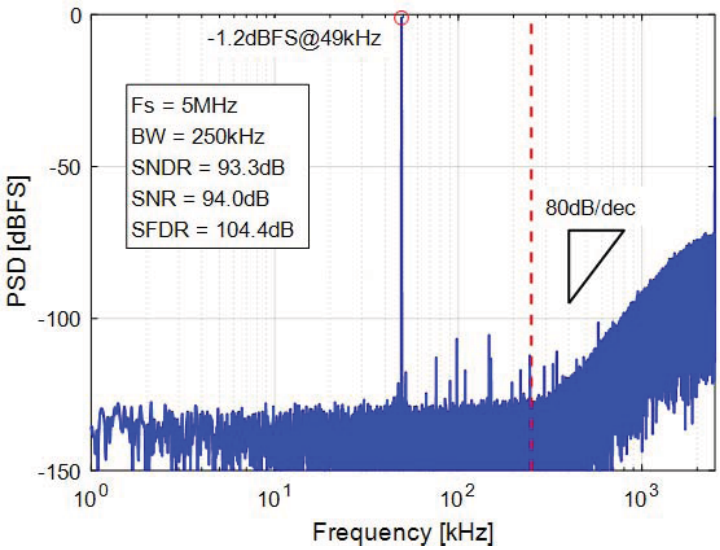

Figure 27.1.4: Measured output spectrum (512k FFT points).

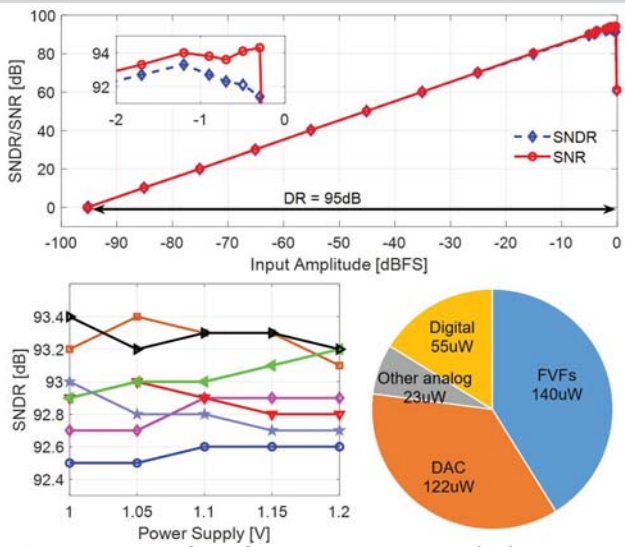

Figure 27.1.5: Measured SNDR/SNR vs. input amplitudes (top); measured SNDR vs. buffer supply across 7 different chips (bottom-left); measured power breakdown (bottom-right).

	ISSCC 16 Shu [2]	ISSCC 17 Liu [7]	ISSCC 20 Liu [8]	ISSCC 20 Tang [3]	ISSCC 20 Jie [6]	This work
Process	55nm	28nm	40nm	40nm	28nm	**40nm**
NS Technique	Closed-loop OTA	Open-loop DA	Passive	Closed-loop DA	Open-loop amp.	**Cap. stack. & dynamic buffering**
NS Order	1	1	1	2	4	**4**
Sharp NTF Across PVT	√	×	×	√	×	√
Supply (V)	1.2	1	1.1	1.1	1	**1.1**
Area (mm^2)	0.072	0.0049	0.061	0.037	0.02	**0.094**
Fs (MS/s)	1	132	2	10	2	**5**
Power (µW)	15.7	460	67.4	107	120	**340**
OSR	500	13.2	25	8	10	**10**
BW (kHz)	1	5000	40	625	100	**250**
SNDR (dB)	101	79.7	90.5	83.8	87.6	**93.3**
DR (dB)	101.7	81.8	94.3	85.5	89	**95**
FoMs (dB)	178.9	180.1	178.2	181.5	176.8	**182**

$$FoMs = SNDR + 10 \cdot \log_{10}\left(\frac{BW}{Power}\right)$$

Figure 27.1.6: Performance summary and comparison.

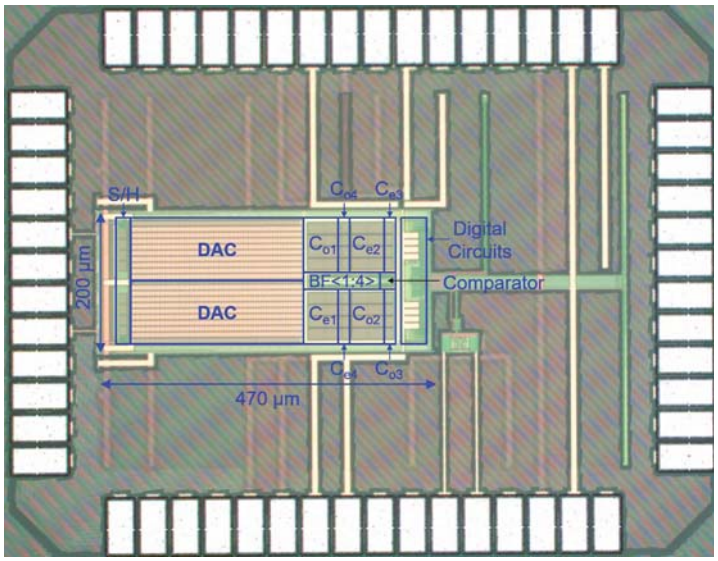

Figure 27.1.7: Die micrograph.

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