# Second-order DAC MES for SAR ADCs

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The successive approximation register (SAR) ADCs suffer from capacitor mismatch when considered for high-precision applications. Recently, a mismatch error shaping (MES) technique suitable for SAR ADCs has been proposed, by which the DAC mismatch error is first-order highpass shaped. The MES technique to the second-order is generalised. A concrete implementation of the second-order MES is presented. Theoretical analysis and simulations verify the feasibility and validity of the proposed technique. Compared to the previous one, the proposed second-order MES shows significantly improved shaping effect.

*Introduction:* Successive approximation register (SAR) ADC is the most energy-efficient ADC architecture with moderate conversion rate and resolution. In recent years, there has been emerging efforts to try to enable the application of SAR ADCs to the regime of high-resolution ΔΣ ADCs. The noise-shaping SAR ADCs, which suppress the comparator and quantisation noise in the signal band, can achieve an effective number of bits (ENOB) of around 13 bit [1, 2]. However, further resolution improvement of SAR ADCs is limited by the non-linearity caused by the DAC mismatch. Dynamic element matching (DEM) [3] and data weighted averaging (DWA) [4] are widely used in multi-bit ΔΣ ADCs to address the mismatch issue; however, the power and area requirements for DEM or DWA increase exponentially with the number of bits, which restrict their applications in SAR ADCs.

In [5], a 12 bit first-order noise-shaping SAR ADC achieving 105 dB spurious-free dynamic range (SFDR) and 101 dB signal to noise and distortion ratio (SNDR) without calibration is presented. This work proposes a mismatch error shaping (MES) technique. The DAC mismatch error is first-order highpass filtered by simply delaying the reset of least significant bit (LSB) capacitor array after sampling. This technique matches the application of SAR ADCs very well, as no additional circuit is needed, and therefore it is not restricted by the number of bits. However, it only achieves first-order shaping effect, and this is insufficient for applications with higher-order noise-shaping and/or larger DAC mismatch errors. In this Letter, we propose a second-order MES technique, by which the mismatch shaping effect is significantly improved.

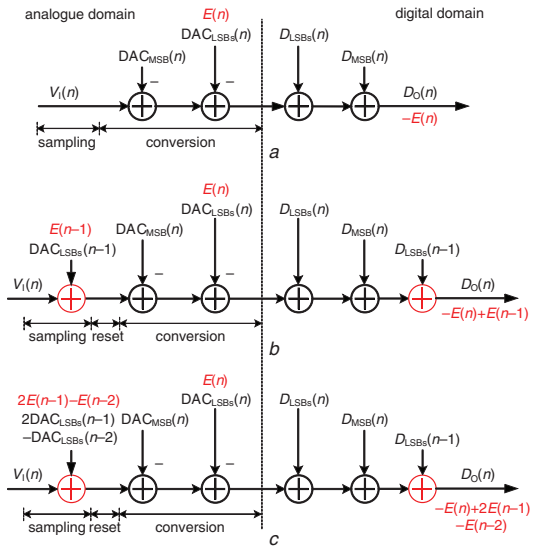


**Fig. 1** *Behavioural model of SAR ADC*

*a* Without MES
*b* With first-order MES
*c* With second-order MES

*Previous first-order MES:* The behavioural model of a classic SAR ADC is shown in Fig. 1*a*. At a conversion cycle of $n$, the input signal $V_I(n)$ is sampled on the DAC in sampling phase and then the analogue weights of MSB and LSB cells, $\mathrm{DAC}_{\mathrm{MSB}}(n)$ and $\mathrm{DAC}_{\mathrm{LSBs}}(n)$, are subtracted from it in the conversion phase. Ignoring the quantisation error and thermal noise (including sampling, comparator, and DAC switch noise), the final residue voltage in analogue domain would be 0. At the same time, the digital output $D_0(n)$ is established from 0 in the digital domain, by adding up the digital weights of MSB and LSB cells, $D_{\mathrm{MSB}}(n)$ and $D_{\mathrm{LSBs}}(n)$. Ideally, the analogue weights of DAC match their digital weights perfectly, and therefore the digital output represents the analogue input accurately. Nevertheless, there is always mismatch between the analogue and digital weights. As a result, non-linearity is unavoidable in the process of conversion. To define the DAC mismatch, the MSB cell can be defined as a reference and its analogue weight is considered equal to its digital weight. Thus, only the LSB cells contain the mismatch error, which is shown as $E(n)$ and appears at the digital domain as $-E(n)$.

Fig. 1*b* explains the first-order MES technique in [5]. In the sampling phase, the analogue weights of LSB cells in the previous cycle, $\mathrm{DAC}_{\mathrm{LSBs}}(n-1)$, is sampled on the DAC together with the input signal $V_I(n)$. Along with $\mathrm{DAC}_{\mathrm{LSBs}}(n-1)$, the DAC mismatch error in the previous cycle, $E(n-1)$, is injected. After a short reset phase, the normal conversion phase continues, and the mismatch error in the present cycle, $E(n)$, is subtracted from the analogue input. In this manner, the total DAC mismatch error introduced in the SAR conversion process is $E(n-1)-E(n)$, which is first-order shaped.

*Proposed second-order MES:* Inspired by the first-order MES, an intuitive idea to realise the second-order MES is injecting a previous mismatch error of $2E(n-1)-E(n-2)$ and using it to cancel the present one $E(n)$. Therefore, the total DAC mismatch would become $-E(n)+2E(n-1)-E(n-2)$ and a second-order shaping effect is obtained. The behavioural model of this idea is shown in Fig. 1*c*. To inject such a previous mismatch error, a combination of LSB analogue weights in previous two cycles, $2\mathrm{DAC}_{\mathrm{LSBs}}(n-1)-\mathrm{DAC}_{\mathrm{LSBs}}(n-2)$, should be added up to the input signal before the SAR ADC conversion phase starts. The basic idea seems simple, but there is no direct path on how to map the equation to hardware implementation as it requires the weighted sum of two previous cycle informations using the same LSB DAC.

This Letter proposes a novel DAC switching scheme that realises the second-order MES. As with the case of first-order MES in [5], the DAC of SAR ADC is segmented into $M$-bit MSB and $N$-bit LSB to mitigate the dynamic range loss. The mismatch error between MSB cells is addressed by the classic DWA [4]. The mismatch error of LSB cells is solved by the proposed second-order MES technique.

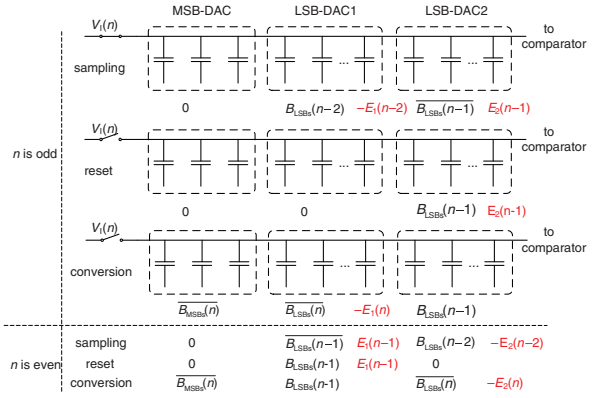


**Fig. 2** *DAC switching scheme of SAR ADC with proposed second-order MES*

An example of the proposed second-order MES operation is illustrated in Fig. 2. In the proposed design, we duplicate the LSB DAC and operate the two LSB-DACs in a ping–pong fashion between odd and even cycles. $B_{\mathrm{MSBs}}$ and $B_{\mathrm{LSBs}}$ are the binary digital weights of MSB and LSB cells, $\overline{B_{\mathrm{LSBs}}}$ represents the complement of $B_{\mathrm{LSBs}}$. $E_1$ and $E_2$ are the mismatch errors of LSB-DAC1 and LSB-DAC2, respectively. In the sampling phase of an odd cycle $n$, $\overline{B_{\mathrm{LSBs}}(n-1)}$ is held on LSB-DAC2, while $B_{\mathrm{LSBs}}(n-2)$ is connected to LSB-DAC1. Along with this operation, $E_2(n-1)-E_1(n-2)$ is injected into the DAC with the input signal. After the sampling switch is disconnected, LSB-DAC1 is reset and LSB-DAC2 switches to $B_{\mathrm{LSBs}}(n-1)$ to inject another $E_2(n-1)$. After all the DAC cells settle, the normal SAR ADC conversion performs on MSB-DAC and LSB-DAC1, and the present mismatch error $E_1(n)$ is injected with the opposite polarity. Finally, the total mismatch error in an odd cycle $n$ is obtained as

$$E_{\mathrm{tot,\,odd}}(n) = -E_1(n) + 2E_2(n-1) - E_1(n-2) \quad (1)$$

Similarly, the total mismatch error of an even cycle $n$ is given by

$$E_{\text{tot, even}}(n) = -E_2(n) + 2E_1(n-1) - E_2(n-2) \quad (2)$$

The DAC mismatch error sequence with the proposed second-order MES is in Table 1, as well as the first-order and second-order integrated error sequences. Since the second-order integrated error sequence is bounded, we conclude that the actual DAC mismatch error, obtained by differentiating the integrated error twice, is second-order shaped.

**Table 1:** DAC mismatch error, first-order, and second-order integrated error sequences with proposed second-order MES

| $n$ | $E_{\text{tot}}$ | $\sum E_{\text{tot}}$ | $\sum\sum E_{\text{tot}}$ |
|---|---|---|---|
| 1 | $-E_1(1)$ | $-E_1(1)$ | $-E_1(1)$ |
| 2 | $-E_2(2) + 2E_1(1)$ | $-E_2(2) + E_1(1)$ | $-E_2(2)$ |
| 3 | $-E_1(3) + 2E_2(2) - E_1(1)$ | $-E_1(3) + E_2(2)$ | $-E_1(3)$ |
| 4 | $-E_2(4) + 2E_1(3) - E_2(2)$ | $-E_2(4) + E_1(3)$ | $-E_2(4)$ |
| 5 | $-E_1(5) + 2E_2(4) - E_1(3)$ | $-E_1(5) + E_2(4)$ | $-E_1(5)$ |
| 6 | $-E_2(6) + 2E_1(5) - E_2(4)$ | $-E_2(6) + E_1(5)$ | $-E_2(6)$ |
| … | … | … | … |

There is also another explanation that helps to understand the proposed second-order MES technique. As is shown in Fig. 2, in a single cycle, only one of the LSB-DACs performs the SAR ADC conversion and the other one is held during the conversion phase. It means that the present mismatch error, $E(n)$, is contributed by only one of the LSB-DACs in a single cycle and can be expressed as

$$E(n) = \begin{cases} E_1(n), & \text{for } n \text{ is odd} \\ E_2(n), & \text{for } n \text{ is even} \end{cases} \quad (3)$$

Therefore, (1) and (2) can be unified as

$$E_{\text{tot}}(n) = -E(n) + 2E(n-1) - E(n-2), \quad (4)$$

which clearly shows the $(1 - z^{-1})^2$ second-order shaping effect.

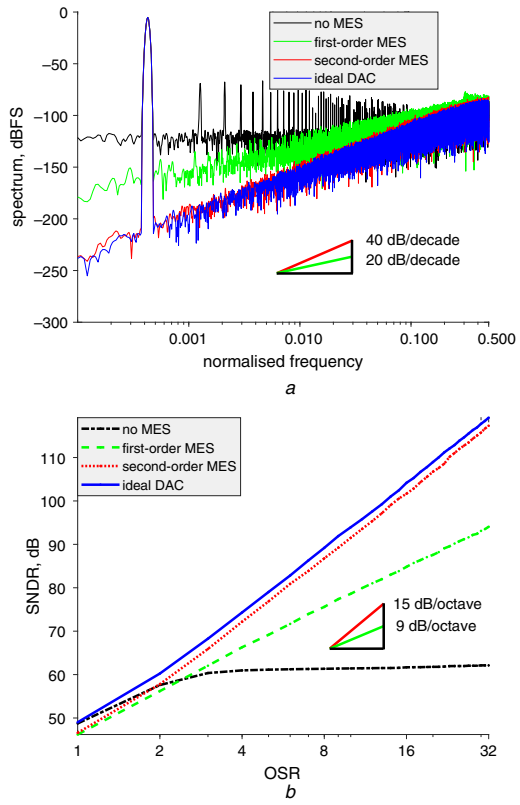


**Fig. 3** *Simulated*

*a* Spectra

*b* SNDRs of noise-shaping SAR ADC with no MES, first-order MES [5], proposed second-order MES, and ideal DAC

*Simulation results:* The proposed second-order MES algorithm is modelled in MATLAB in the context of a 10 bit second-order noise-shaping SAR ADC with noise transfer function (NTF) = $(1 - z^{-1})^2$. The DAC of the SAR ADC is segmented into 3 bit MSB and 7 bit LSB. The unit DAC cell is assumed to be normally distributed with a 5% standard deviation.

In Fig. 3, we compare the output spectra and SNDRs of the noise-shaping SAR ADC with no MES, first-order MES, second-order MES, and ideal DAC. It shows that both MES techniques can eliminate the distortion terms caused by the DAC mismatch error. However, the first-order MES is not sufficient for this second-order noise-shaping SAR ADC, its spectrum and SNDR show 20 dB/decade and 9 dB/octave slope, respectively. By contrast, the proposed second-order MES enables the 40 dB/decade spectrum slope and 15 dB/octave SNDR slope, and the SNDR improvement is 17 dB at oversampling ratio (OSR) = 16. The performance of the second-order MES is very close to that of the ideal DAC.

*Conclusion:* In this Letter, we propose a second-order MES technique for noise-shaping SAR ADCs. With this technique, the DAC mismatch error can be second-order shaped. Compared to the previous first-order MES, the proposed one shows significantly improved shaping effect. It is particularly useful when high linearity and small area are demanded, but the device mismatch is large.

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One or more of the Figures in this Letter are available in colour online.

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## References

1 Liu, C.C., and Huang, M.C.: 'A 0.46 mW 5 MHz-BW 79.7 dB-SNDR noise-shaping SAR ADC with dynamic-amplifier-based FIR-IIR filter'. IEEE Int. Solid-State Circuits Conf. (ISSCC), San Francisco, CA, USA, February 2017, pp. 466–467

2 Guo, W., Zhuang, H., and Sun, N.: 'A 13b-ENOB 173 dB-FoM second-order NS SAR ADC with passive integrators'. IEEE Symp. VLSI Circuits (VLSI-Circuits), Kyoto, Japan, June 2017

3 Van De Plassche, R.J.: 'Dynamic element matching for high-accuracy monolithic D/A converters', *J. Solid-State Circuits*, 1976, **11**, (6), pp. 795–800

4 Baird, R.T., and Fiez, T.S.: 'Improved ΔΣ DAC linearity using data weighted averaging'. IEEE Int. Symp. Circuits and Systems, Seattle, WA, USA, May 1995, vol. 1, pp. 13–16

5 Shu, Y.S., Kuo, L.T., and Lo, T.Y.: 'An oversampling SAR ADC with DAC mismatch error shaping achieving 105 dB SFDR and 101 dB SNDR over 1 kHz BW in 55 nm CMOS', *J. Solid-State Circuits*, 2016, **51**, (12), pp. 2928–2940