A 0.029-mm^2 17-fJ/Conversion-Step Third-Order CT ΔΣ ADC With a Single OTA and Second-Order Noise-Shaping SAR Quantizer

Jiaxin Liu, *Student Member, IEEE*, Shaolan Li, *Student Member, IEEE*, Wenjuan Guo, *Member, IEEE*, Guangjun Wen, *Senior Member, IEEE*, and Nan Sun, *Senior Member, IEEE*

***Abstract*— This paper presents a compact and power efficient third-order continuous-time (CT) delta-sigma (ΔΣ) analog-to-digital converter (ADC) with a single operational transconductance amplifier (OTA). A 4-bit second-order fully passive noise-shaping (NS) successive-approximation-register (SAR) ADC is employed as the quantizer while inherently provides two additional NS orders. Fabricated in 40-nm CMOS, the prototype occupies 0.029 mm^2 of active area and consumes 1.16 mW of power when clocked at 500-MHz sampling frequency. The proposed CT ΔΣ ADC achieves a peak signal-to-noise-and-distortion ratio (SNDR) of 70.4 dB over 12.5-MHz bandwidth, yielding a Walden figure of merit (FoM) of 17 fJ/conversion-step.**

***Index Terms*— Analog-to-digital converter (ADC), coefficient scaling, continuous-time (CT) delta-sigma (ΔΣ) ADC, excess loop delay compensation (ELDC), hybrid ADC, low-noise and high-speed comparator, passive noise shaping (NS), successive approximation register (SAR).**

I. Introduction

THE continuous time (CT) delta-sigma ΔΣ analog-to-digital converter (ADC) is a suitable architecture for high-resolution, low-power, and wide-bandwidth applications. Comparing to its discrete-time (DT) counterpart, the CT ΔΣ ADC is preferred owing to its relaxed integrator settling requirement and inherent anti-alias filtering capability. A typical CT ΔΣ ADC is shown in Fig. 1(a), which consists of a loop filter, a feedback digital-to-analog converter (DAC), and a quantizer. There are three common ways to boost the signal-to-quantization-noise ratio (SQNR) of a ΔΣ ADC. First, the oversampling ratio (OSR) can be enlarged by increasing the sampling frequency f_s; however, this directly increases the power consumption. Second, the loop filter order can be increased to achieve more aggressive noise shaping (NS), but this comes with the cost of increased circuit complexity and degraded loop stability. The third approach is to increase the quantizer resolution, but it comes with its own limitation. A flash quantizer is often limited to 4 bit because its hardware cost (power, area, and complexity) increases exponentially with the number of bits [1]–[3]. By contrast, a successive approximation register (SAR) quantizer is more energy efficient for moderate resolution as its hardware cost scales linearly with the number of bits. However, when used inside a wideband closed-loop ΔΣ ADC, the SAR quantizer resolution is limited to 6 bit or below due to its speed constraint [4]–[10].

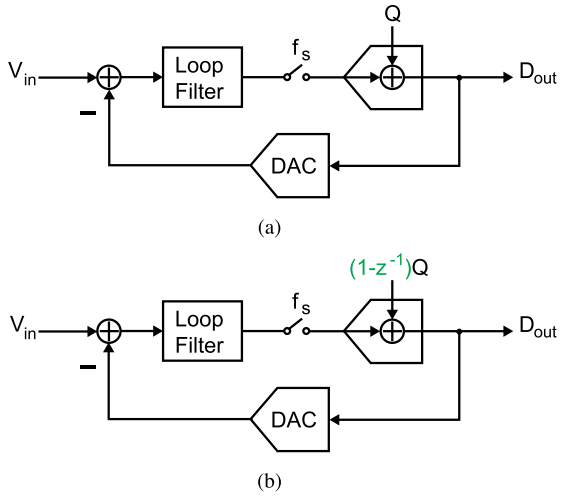


Fig. 1. (a) Typical CT ΔΣ ADC. (b) CT ΔΣ ADC with a NS quantizer.

An effective solution to address the quantizer resolution limitation is to embed NS capability inside the quantizer. This way, the quantizer can achieve higher in-band resolution with a relatively small nominal resolution. A model of a CT ΔΣ ADC with a first-order NS quantizer is shown in Fig. 1(b).

Manuscript received July 21, 2018; revised October 8, 2018; accepted October 31, 2018. Date of publication November 23, 2018; date of current version January 25, 2019. This paper was approved by Associate Editor Jeffrey Gealow. This work was supported by NSF under Grant 1254459, Grant 1509767, and Grant 1527320. *(Corresponding author: Nan Sun.)*

J. Liu is with School of Information and Communication Engineering, University of Electronic Science and Technology of China, Chengdu, Sichuan 611731 China. He was with Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, TX 78712 USA. He is also with Department of Electronic Engineering, Tsinghua University, Beijing 100084 China.

S. Li, W. Guo, and N. Sun are with the Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, TX 78712 USA (e-mail: nansun@mail.utexas.edu).

G. Wen is with the School of Information and Communication Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2018.2879955

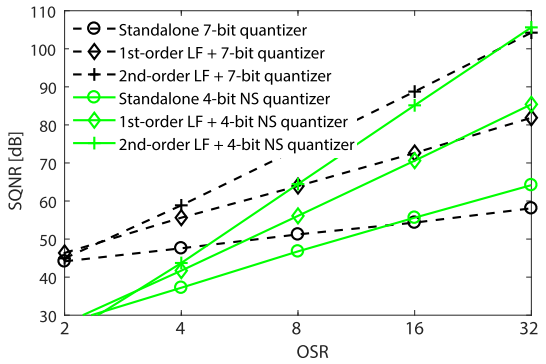


Fig. 2. Simulated SQNRs with conventional and NS quantizers.

Comparing to Fig. 1(a), the difference is that the quantization error in Fig. 1(b) is shaped before injecting into the main loop. Fig. 2 shows the simulated SQNRs of a 7-bit conventional quantizer and a 4-bit NS quantizer as well as the cases of embedding them in a first-order and second-order loop filters. It can be seen that the 4-bit NS quantizer can outperform the 7-bit conventional quantizer by oversampling, owing to its inherent NS capability. With the additional NS order provided by the quantizer, the requirement on the loop filter order, the sampling frequency, and the quantizer nominal resolution of the $\Delta\Sigma$ ADC can be greatly relaxed. Having said that an NS quantizer does not come for free; however, as long as its cost can be made small, it is an attractive alternative to boost the ADC resolution.

Due to their merits, there have been emerging efforts in the research community to develop novel NS quantizers [11]–[21]. The noise-shaped integrating quantizer (NSIQ) proposed in [11] achieved first-order NS, but it requires an active operational transconductance amplifier (OTA). Thus, the total number of OTAs in the $\Delta\Sigma$ ADC is unchanged; it is still the same as the noise transfer function (NTF) order. Moreover, it requires a fast counting clock whose frequency increases exponentially with the resolution. Although the speed and resolution tradeoff can be alleviated by incorporating a digital back-end integrator as in [12], the G_m–C integrator inside the quantizer requires calibration to ensure robustness against process, voltage, and temperature (PVT) variations. To obviate the need for OTAs that are scaling incompatible and power hungry, voltage-controlled oscillator (VCO)-based NS quantizer has been proposed in [13]–[19]. It is mostly digital and thus scaling friendly. Moreover, in addition to the first-order NS, it can bring intrinsic dynamic element matching (DEM) capability [13]–[15]. Nevertheless, the VCO's voltage-to-frequency gain is highly nonlinear and sensitive to PVT variation. Note that the NSIQ and the VCO quantizer can be combined to achieve second-order NS and 6-bit nominal resolution, therefore significantly improving the quantizer resolution [20]. Yet, additional non-idealities, including leakage from both quantizers and their gain mismatches, degrade the overall performance. It requires a delay-locked loop for tuning, but this increases the circuit complexity. Recently, a first-order NS SAR quantizer in a DT $\Delta\Sigma$ ADC is proposed in [21]. This SAR-based NS quantizer is fully passive, OTA-free, and PVT robust. However, with an NTF zero at 0.5, its NS capability is rather limited. It can only provide 9.5-dB in-band SQNR improvement.

This paper presents a third-order CT $\Delta\Sigma$ ADC with a novel second-order NS SAR quantizer. Comparing to a conventional second-order passive DT loop filter with SAR quantizer, the NS SAR quantizer is simpler and more power efficient, for it uses the same capacitor array for multi-bit quantization, digital-to-analog conversion, and analog subtraction. This NS SAR quantizer also has several key advantages over the prior NS quantizers for $\Delta\Sigma$ ADCs. First, its circuit is simple, as it requires only a few extra switches, capacitors, and comparator input pairs on top of a standard SAR ADC. Second, it is OTA-free and scaling friendly. Third, the quantizer NTF is set by component ratios, and thus, is robust against PVT variation and is calibration-free. Fourth, it achieves the second-order NS with the NTF of $(1-0.75z^{-1})^2$ and provides 24-dB in-band SQNR improvement. Finally, the excess loop delay compensation (ELDC) can be easily embedded inside it, which reduces the overall circuit complexity. Moreover, comparing to the prior standalone second-order NS SAR ADC in [22], the proposed NS SAR quantizer has two clear merits. First, it significantly reduces the kT/C noise. Thus, for the same thermal noise budget, the total capacitance can be reduced by 2.4×, leading to substantial area and power saving. The capacitance reduction also shortens the DAC settling time, speeding up the quantizer operation. Second, the comparator noise requirement is relaxed, resulting in over 40% reduction in the comparator power.

Owing to the inherent second-order NS capability of the quantizer, the proposed CT $\Delta\Sigma$ ADC achieves an overall third-order NS with the NTF of $(1-z^{-1})(1-0.75z^{-1})^2$ but requiring only a single OTA. As a result, the overall circuit power and complexity are reduced. The loop stability is also improved. Because two NS orders are realized in the DT domain using switched capacitors inside the quantizer, they are insensitive to PVT variations. As a result, the overall stability of the proposed third-order CT $\Delta\Sigma$ ADC is similar to that of a first-order CT $\Delta\Sigma$ ADC when considering the RC variation. From a different angle, the proposed $\Delta\Sigma$ ADC can also be viewed as a CT-DT hybrid with the one-order NS realized in CT and two-order NS realized in DT. It combines the merits of CT $\Delta\Sigma$ ADCs, which are anti-alias filtering capability and low power, with the merit of DT $\Delta\Sigma$ ADCs, which is PVT robustness. A prototype chip is realized in 40-nm CMOS with an active area of only 0.029 mm^2. It achieves a peak signal-to-noise-and-distortion ratio (SNDR) of 70.4 dB over 12.5-MHz bandwidth while consuming only 1.16 mW of power, leading to a competitive Walden figure of merit (FoM) of 17 fJ/conversion-step.

This paper provides the detailed analyses and implementation of the proposed CT $\Delta\Sigma$ ADC. It is a significant extension of [23] and is organized as follows. Section II discusses the proposed second-order NS SAR quantizer. Section III presents the proposed CT $\Delta\Sigma$ ADC. Section IV provides the measurement results. Finally, Section V concludes this paper.

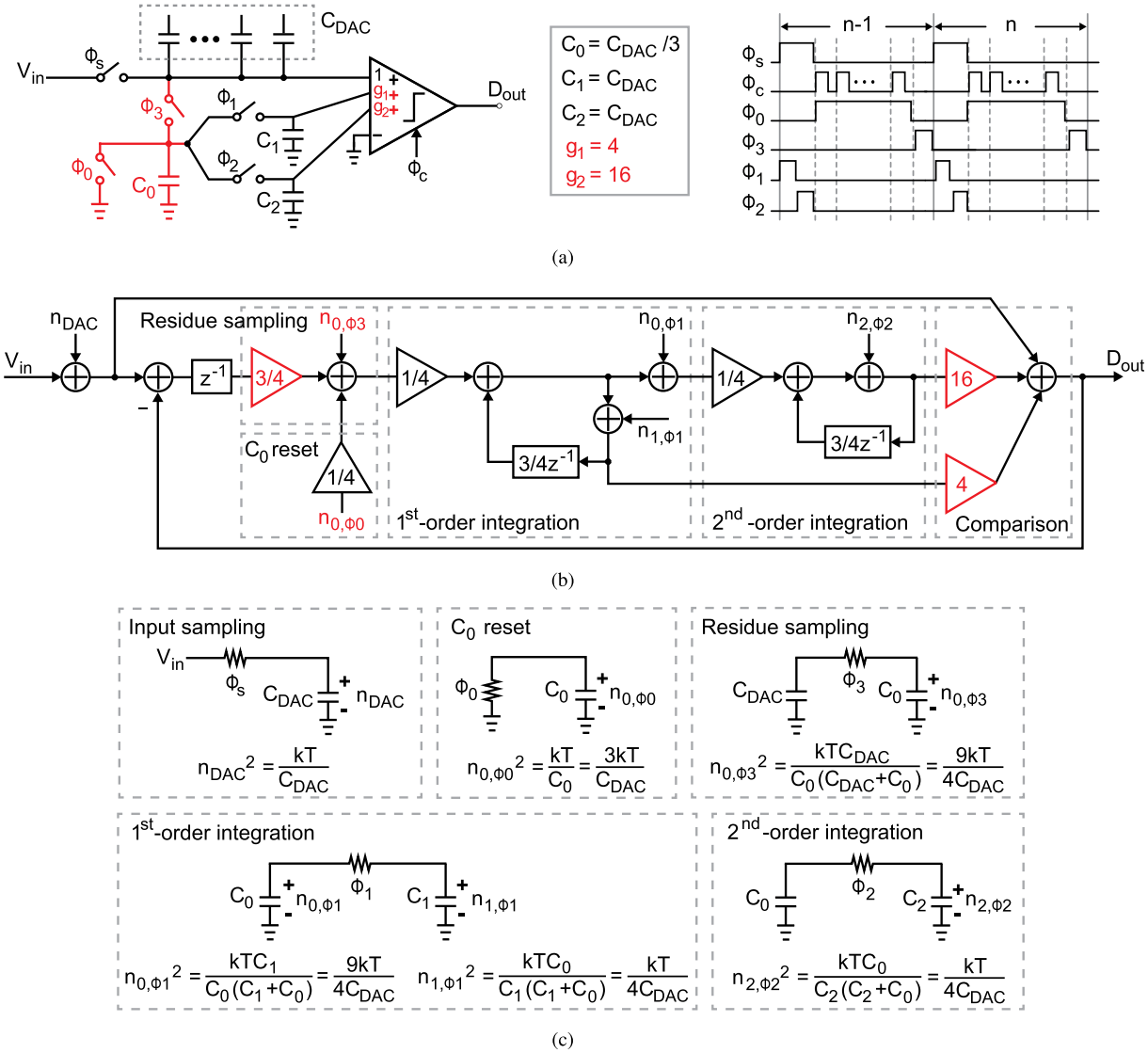


Fig. 3. Prior NS SAR ADC [22]. (a) Simplified schematic and timing. (b) Signal flow diagram with kT/C noise. (c) Noise definition and calculation.

II. Proposed Second-Order NS SAR Quantizer

A. Brief Review of NS SAR ADCs

The NS SAR ADC is an emerging ADC architecture that aims to combine the benefits of both SAR and $\Delta\Sigma$ ADCs while simultaneously obviating their drawbacks [22], [24]–[31]. The works of [24]–[26] use OTA to build active filters and realize aggressive NTF, however at the cost of OTA's large power consumption and scaling unfriendliness. The works of [30] and [31] use dynamic amplifiers to replace OTAs to reduce both power and noise. Nevertheless, the gain of a dynamic amplifier is sensitive to PVT variations. Digital background calibration can be used to ensure PVT robustness, but it increases the design complexity and requires many input samples for convergence [31]. Alternatively, a few recent works propose to use switched capacitors to build fully passive filters [22], [27]–[29]. They are simple, OTA free, and scaling friendly. Moreover, their NTF is set by component ratio, and thus, is accurate and calibration free. Comparing to OTA-based active filters, the limitation for using lossy passive filters is that the NTF zeros cannot be placed at the unit cycle. In addition, passive filters do not provide voltage gain, and hence, the comparator noise suppression is not as effective. Yet, a fully passive NS SAR is well suited as an NS quantizer for $\Delta\Sigma$ ADCs. Its merits of simplicity, low power, and PVT robustness are maintained, while its limitations are easily addressed by placing it after an active *RC* filter. The front-end filter provides gain and sufficient suppression for both the quantization error and the comparator noise.

B. Prior Second-Order NS SAR ADC of [22]

Fig. 3(a) shows the simplified core schematic of the prior standalone second-order NS SAR ADC of [22]. Four switches ($\phi_0 - \phi_3$) and three capacitors ($C_0 - C_2$) are added on top of a standard SAR ADC to implement the passive integrators. At the end of a complete SAR conversion, the residue voltage on C_{DAC} is sampled on a small capacitor, $C_0 = C_{\mathrm{DAC}}/3$, and then sequentially merged with two capacitors, $C_1 = C_2 = C_{\mathrm{DAC}}$, for passive integrations. Signal attenuations happen due to the charge sharing operations, which are $C_{\mathrm{DAC}}/(C_{\mathrm{DAC}} + C_0) = 3/4$ by residue

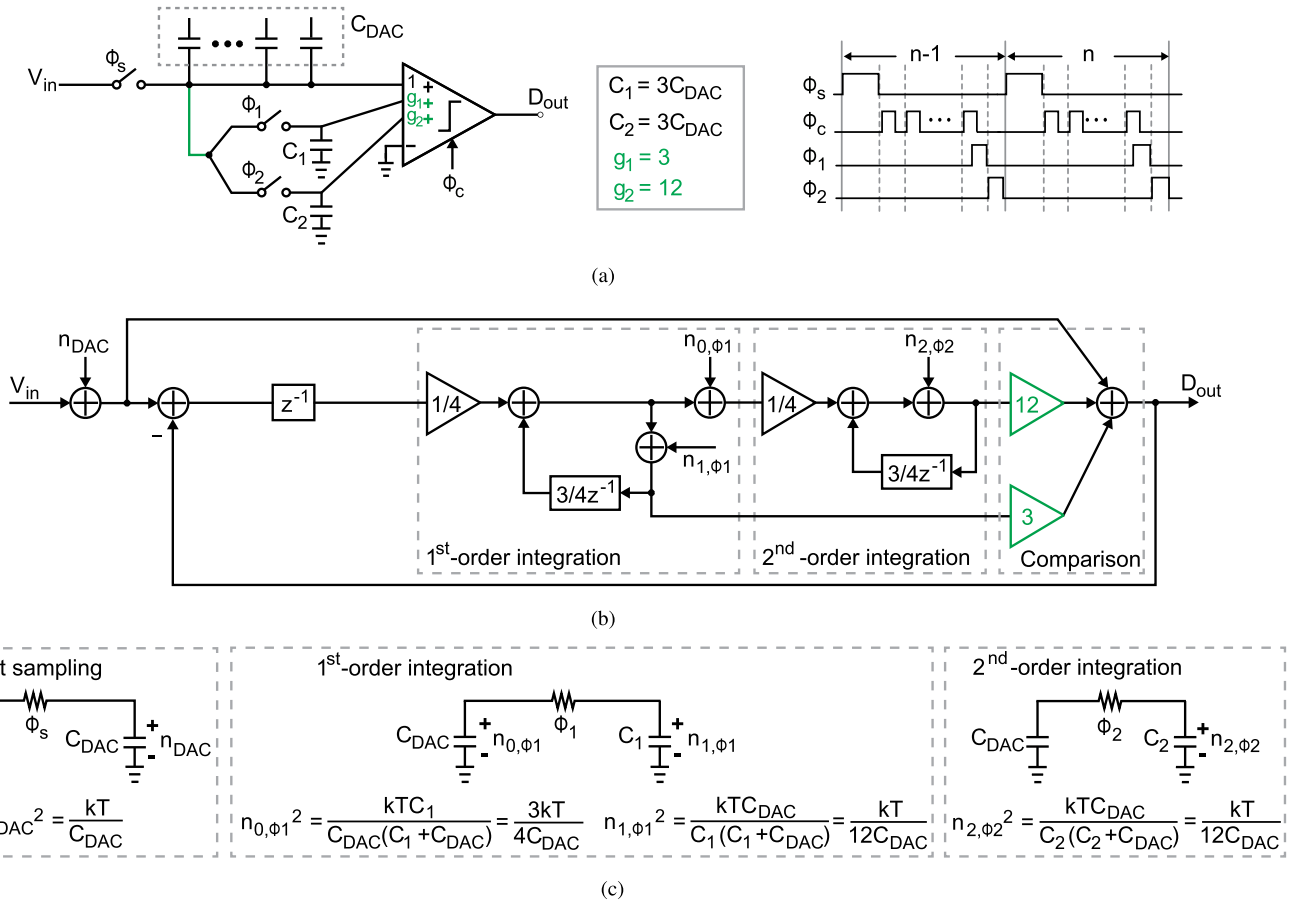


Fig. 4. Proposed NS SAR ADC. (a) Simplified schematic and timing. (b) Signal flow diagram with kT/C noise. (c) Noise definition and calculation.

sampling and $C_0/(C_0 + C_{1,2}) = 1/4$ by each passive integration. A three-input-pair comparator works as a dynamic adder in the feed-forward path. The three input pairs are sized with the ratio of 1:4:16 to provide the passive gains, g_1 and g_2, to compensate for the signal attenuations. The NTF zeros of the NS SAR ADC are determined by the ratios of C_0 to C_1 and C_2, which are $z = C_{1,2}/(C_0 + C_{1,2}) = 3/4$. The resulted NTF of the NS SAR ADC is $(1 - 0.75z^{-1})^2$.

The residue sampling on C_0 results in two significant disadvantages. One is the signal attenuation of 3/4 as mentioned earlier. The other is the greatly increased kT/C noise. Fig. 3(b) shows the signal flow diagram of the NS SAR ADC with kT/C noise. The overall input referred kT/C noise can be calculated as

$$n_{\text{tot}} = n_{\text{DAC}} + \left(n_{0,\phi 3} + \frac{1}{4}n_{0,\phi 0}\right)\left(2 - \frac{3}{4}z^{-1}\right) + 4n_{1,\phi 1} + 4n_{0,\phi 1}\left(1 - \frac{3}{4}z^{-1}\right) + 16n_{2,\phi 2}\left(1 - \frac{3}{4}z^{-1}\right). \quad (1)$$

The above-mentioned noise expressions are in amplitude. The quadratic expression of every noise source is defined and shown in Fig. 3(c). Note that $n_{0,\phi 1}$ and $n_{1,\phi 1}$ are from the same clock phase. They are correlated but with the opposite sign. The other noise sources are independent.

C. Proposed Second-Order NS SAR ADC

The proposed second-order fully passive NS SAR ADC is shown in Fig. 4(a). Comparing to [22], the proposed NS SAR has lower circuit complexity. It adds only two switches and two capacitors on top of a standard SAR ADC. The proposed scheme obviates the residue sampling on C_0 in Fig. 3(a); instead, it directly connects C_{DAC} to two large capacitors C_1 and C_2 for integrations, where $C_1 = C_2 = 3C_{\text{DAC}}$. Even though this modification seems small, it brings two key advantages. First, it removes the signal attenuation of 3/4 due to the residue sampling on C_0. To realize the same NTF of $(1 - 0.75z^{-1})^2$, the comparator input pair ratio can be reduced from 1:4:16 of [22] to 1:3:12 of the proposed work. The relaxed comparator gain requirement leads to reduced comparator power. For the same comparator input referred noise budget, the proposed scheme reduces the comparator power by more than 40%. Second, it removes two large kT/C noise sources due to C_0 reset and residue sampling, which are $n_{0,\phi 0}$ and $n_{0,\phi 3}$ in Fig. 3(b).

The signal flow diagram and noise calculation of the proposed NS SAR ADC are shown in Fig. 4(b) and (c). For the proposed NS SAR scheme, the overall input referred kT/C noise is given by

$$n_{\text{tot}} = n_{\text{DAC}} + 3n_{1,\phi 1} + 3n_{0,\phi 1}\left(1 - \frac{3}{4}z^{-1}\right) + 12n_{2,\phi 2}\left(1 - \frac{3}{4}z^{-1}\right). \quad (2)$$

Comparing to (1), the noise sources of $n_{0,\phi 3}$ and $n_{0,\phi 0}$ are eliminated. In addition, the coefficients for $n_{1,\phi 1}$, $n_{0,\phi 1}$, and

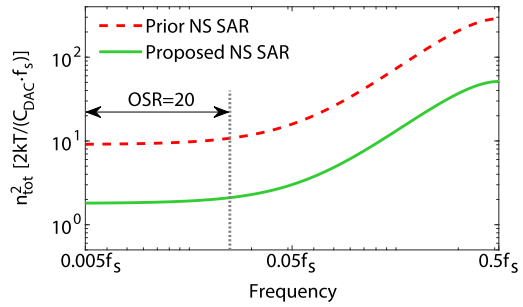


Fig. 5. Input referred overall kT/C noise PSDs.

TABLE I
CAPACITOR VALUES FOR THE SAME OVERALL kT/C NOISE BUDGET

	C_{DAC}	C_0	C_1	C_2	Total
Prior work [22]	C	C/3	C	C	10C/3
Proposed work	C/5	-	3C/5	3C/5	7C/5

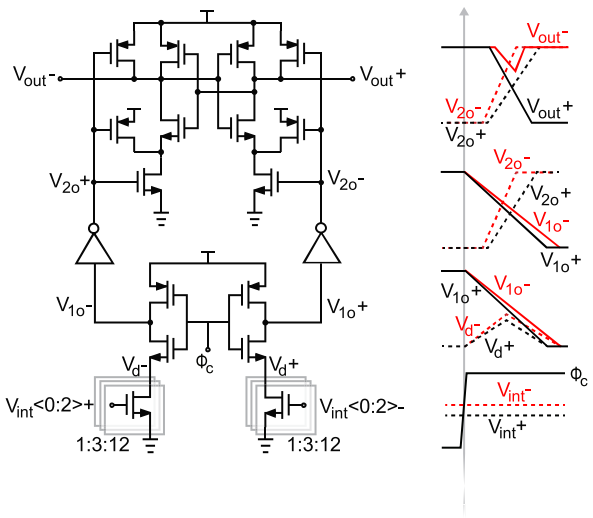


Fig. 6. Schematic of the proposed three-stage three-input-pair comparator.

$n_{2,\phi 2}$ in (1) are scaled by 3/4 in (2), leading to the over 40% noise power reduction.

Fig. 5 compares the total input referred kT/C noise power spectral densities (PSDs) of the prior NS SAR of [22] with the proposed NS SAR. Both PSDs are flat in-band. The in-band PSDs of the prior and the proposed NS SAR schemes are 18 kT/($C_{\mathrm{DAC}} \cdot f_s$) and 3.6 kT/($C_{\mathrm{DAC}} \cdot f_s$), respectively. Thus, for the same C_{DAC}, the proposed architecture reduces the kT/C noise by 5×. From a different perspective, for the same total kT/C noise budget, the proposed NS SAR architecture can use a five-time smaller C_{DAC}. This relaxes the quantizer driver requirement and the power consumption. It also reduces the DAC switching power and settling time. Table I summarizes the capacitor values used by the two NS SAR architectures for the same kT/C noise budget. The total capacitance of the proposed NS SAR quantizer is 2.4× smaller than that of the prior NS SAR of [22], which is a significant area saving. Note that because C_{DAC} has to be partitioned into smaller unit capacitors, its capacitance density is smaller than that for lump capacitors $C_0 - C_2$, and thus, the actual area saving in real implementation is even larger.

In addition, a minor drawback of the proposed NS SAR scheme is that the two passive integrations cannot be done within the sampling phase as in [22], thus more clock cycles are required. However, as long as the comparison result of last bit is determined, the first-order integration can start. In this manner, the first-order integration phase Φ_1 can be merged with the remaining time for DAC feedback of the last bit cycle. Therefore, the clock cycle for Φ_1 is saved and only one extra cycle for Φ_2 is required, as shown in Fig. 4(a). Moreover, considering that the proposed scheme greatly relaxes the DAC settling requirement by reducing the capacitor size, the overall ADC operation speed may not be slowed.

D. Proposed Three-Input-Pair Comparator

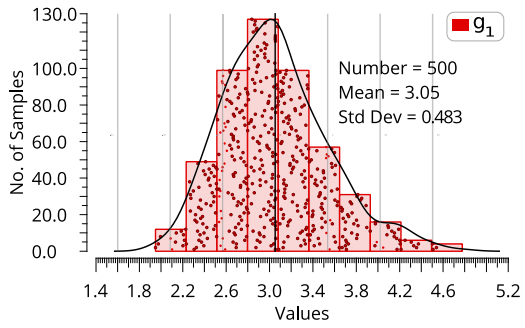
Fig. 6 presents the schematic of the proposed three-stage three-input-pair dynamic comparator[1] used in the NS SAR quantizer, the waveforms of key nodes are also sketched alongside. The width ratios of the three input pairs are set to 1:3:12, which realizes the relative path gains, $g_1 = 3$ and $g_2 = 12$, as shown in Fig. 4(b). When at clock rising edges, the transient signal jumps of the drains and sources of input pairs can be coupled to input through the gate–drain and gate–source capacitance, resulting in kickback noise. For the StrongArm latch-based comparator as in [22], both the gate–source and gate–drain couplings result in kickback noise, and the drains experience rail-to-rail signal jumps. In the proposed design, the sources of input pairs are grounded, thereby removing the kickback due to gate–source coupling [32]; it only suffers from the kickback by the gate–drain coupling, and the drain jumps are only a fraction of the rail-to-rail swing. As a result, the arrangement in the proposed comparator reduces the kickback noise. In addition, it removes the dependence of the source voltage on the gate voltage, making the path gains g_1 and g_2 to be first-order independent of the input differential-mode voltages. The two inverters connecting V_{1o} and V_{2o} comprise the comparator second stage. They act as dynamic amplifiers and serve as the intermediate buffer between the first-stage pre-amplifier and the last-stage latch, reducing the loading of the first stage and accelerating the comparison speed. They also provide extra voltage gain, reducing the noise and the offset from the latch, as well as shortening the time needed for the latch regeneration. The inverter outputs are applied to the latch stage as both input and clock signals. As a result, the proposed comparator requires only one clock at the first stage, relaxing the clock path driving requirement.

[1]In Fig. 4, of the prior conference paper [23], the V_{1o+}/V_{1o-} connections of the comparator are wrongly drawn.

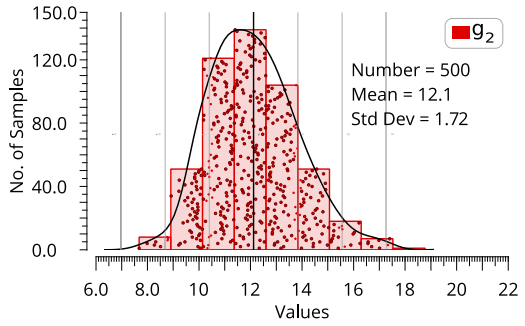
E. Robustness of Proposed NS SAR Against PVT Variations

To analyze the robustness of the proposed second-order NS SAR ADC, let us examine its NTF. With $C_1 = C_2 = 3C_{\mathrm{DAC}}$ as mentioned earlier, the NTF can be derived and shown in the following:

$$\mathrm{NTF}(z) = \frac{\left(1 - \frac{3}{4}z^{-1}\right)^2}{1 + \left(\frac{g_1}{4} + \frac{g_2}{16} - \frac{3}{2}\right)z^{-1} + \left(\frac{9}{16} - \frac{3g_1}{16}\right)z^{-2}}. \quad (3)$$



(a)



(b)

Fig. 7. MC simulation results of (a) g_1 and (b) g_2.

Since the NTF zeros are solely set by capacitor ratios, their locations are insensitive to PVT variations. The pole locations, however, depend on not only capacitor ratios but also g_1 and g_2. g_1 and g_2 represent relative strengths of the comparator input pairs. They are first-order set by transistor width ratios, and hence, are not sensitive to process corner, voltage, and temperature variations. Yet, g_1 and g_2 can change due to random mismatches in the transistor threshold voltages. The transistor threshold mismatch can be suppressed by enlarging the transistor size; however, this comes with the cost of increased comparator power and kickback noise. To balance these tradeoffs, the comparator input pair sizes in the prototype ADC are chosen to be 0.24 μm/0.04 μm, 0.72 μm/0.04 μm, and 2.88 μm/0.04 μm, respectively. Under this condition, the 500-run Monte Carlo (MC) SPICE simulation results for g_1 and g_2 are plotted in Fig. 7. It can be seen that the mean values of g_1 and g_2 are close to 3 and 12, respectively. Their standard deviations are 0.48 and 1.7, respectively.

To ensure the stability of the NS SAR, the NTF poles need to be within the unity circle, which translates to the stability condition of $7g_1 + g_2 \leq 49$. It is shown in Fig. 8, together with the scatter plots of g_1 and g_2. It can be seen that they are within the stable region, indicated as the green dotted area. If more margins are needed, the nominal values for g_1 and g_2 can be downward shifted from 3 and 12 to 2.5 and 10, respectively. This comes with a small SQNR penalty of 1.5 dB. The other option is to enlarge the transistor sizes, as mentioned earlier.

Because g_1 and g_2 variations only slightly alter the location of NTF poles, their influence on the overall ADC SQNR

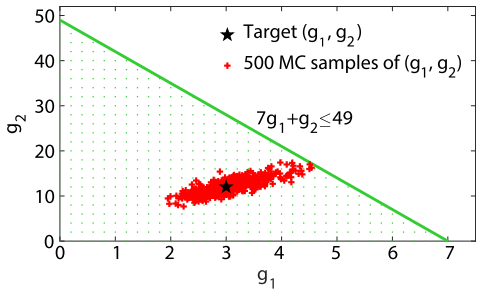


Fig. 8. Stability condition and scatter plot of g_1 and g_2.

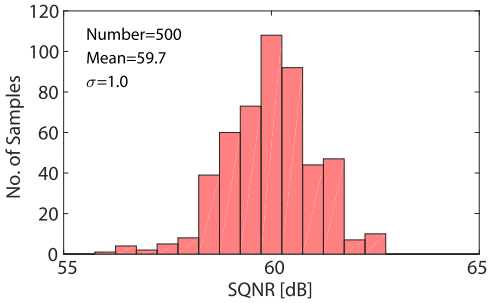


Fig. 9. MC simulation result of the proposed NS SAR ADC.

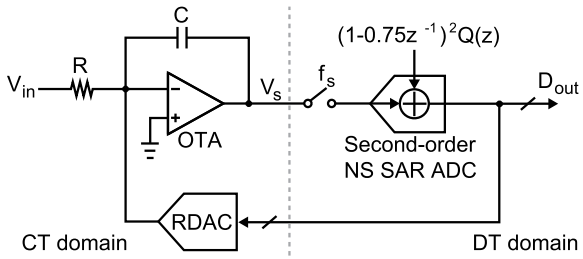


Fig. 10. Basic architecture of the proposed third-order CT ΔΣ ADC with the second-order NS SAR quantizer.

is limited. Fig. 9 shows the simulated SQNR distribution of a 4-bit second-order NS SAR ADC at the OSR of 20, based on the g_1 and g_2 values from the 500-run MC simulation results of Fig. 7. The mean SQNR is 59.7 dB, while the standard deviation is only 1 dB, which demonstrates the robustness of the proposed NS SAR ADC architecture. The fundamental reason for its robustness is that the NTF poles and zeros are the first-order set by capacitor and transistor size ratios, which are insensitive to PVT variations.

III. Proposed CT ΔΣ ADC With NS SAR Quantizer

A. CT-DT Hybrid Architecture

The basic idea of the proposed third-order ΔΣ ADC is depicted in Fig. 10. It is a CT-DT hybrid. The CT portion shown on the left-hand side of Fig. 10 includes an active *RC* integrator and a 4-bit non-return-to-zero (NRZ) resistor DAC (RDAC). The DT portion, shown on the right-hand side of Fig. 10, is the proposed NS SAR.

The *RC* integrator realizes the CT transfer function of $1/s$, it can be translated into the z-domain as $z^{-1}/(1-z^{-1})$.

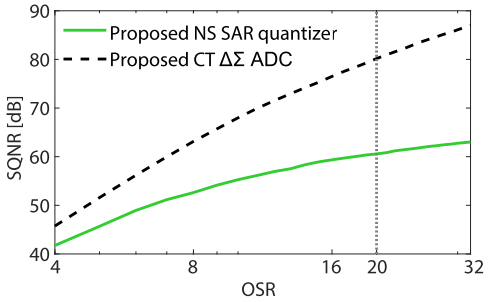


Fig. 11. Simulated SQNRs of the CT $\Delta\Sigma$ ADC and the NS SAR quantizer.

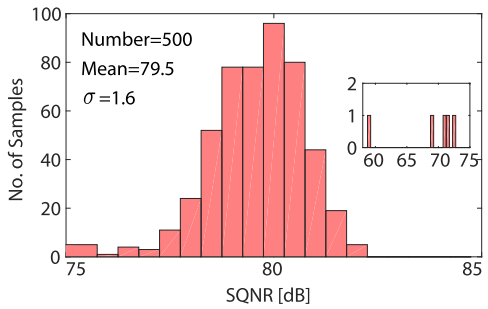
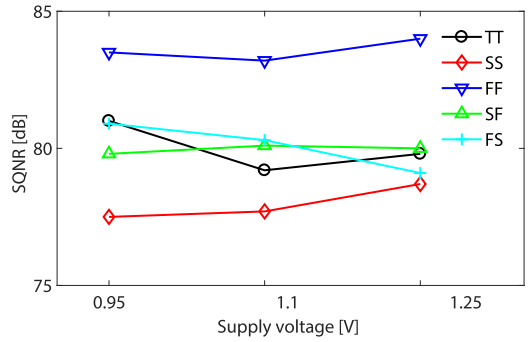
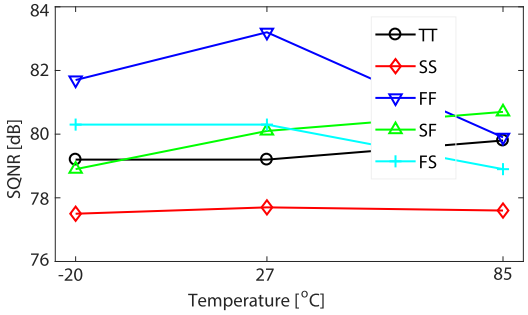


Fig. 12. MC simulation result of the proposed CT $\Delta\Sigma$ ADC.



(a)



(b)

Fig. 13. Simulated SQNRs of the CT $\Delta\Sigma$ ADC (a) with supply voltage and process corner variations and (b) with temperature and process corner variations.

Combining with the $(1-0.75z^{-1})^2$ second-order shaping by the NS quantizer, the overall NTF of proposed CT $\Delta\Sigma$ ADC is

$$\text{NTF} = (1-z^{-1})(1-0.75z^{-1})^2. \tag{4}$$

Taking advantage of the second-order NS capability provided by the NS SAR quantizer, the CT loop filter is greatly simplified. Even though the overall $\Delta\Sigma$ ADC is third order, it requires only a single OTA. Furthermore, the CT-DT hybrid architecture combines the merits of both CT and DT $\Delta\Sigma$ ADCs. CT $\Delta\Sigma$ ADC has anti-alias filtering capability and reduces OTA power by relaxing its settling requirement; however, its loop filter response is sensitive to RC product variation. By contrast, the DT $\Delta\Sigma$ ADC's NTF is robust against PVT variations, but it is less power efficient and does not have anti-alias filtering capability. The proposed CT-DT hybrid maintains anti-alias filtering capability and low-power consumption of the front-end OTA by operating it in the CT domain, and at the same time, benefits from the PVT robustness of the DT second-order NS SAR quantizer. Because it has only one active RC filter, the robustness of the proposed third-order $\Delta\Sigma$ ADC is similar to that of a first-order CT $\Delta\Sigma$ ADC. Its robustness against RC product variation is higher than that of a third-order purely CT $\Delta\Sigma$ ADC.

Fig. 11 shows the simulated SQNR of the proposed third-order $\Delta\Sigma$ ADC and the proposed second-order NS SAR quantizer. At the OSR of 20, the second-order NS SAR quantizer itself already achieves 60-dB SQNR. Placing this NS SAR quantizer inside a first-order CT loop filter, the overall third-order $\Delta\Sigma$ ADC achieves 80-dB SQNR.

Fig. 12 shows the SQNR distribution of the proposed $\Delta\Sigma$ ADC based on the g_1 and g_2 values from the 500-run MC simulation results of Fig. 7. Overall, the mean value of the SQNR distribution is 79.5 dB with a standard deviation of 1.6 dB. It can be seen that 99% samples achieve SQNR beyond 75 dB.

Fig. 13(a) shows the simulated SQNRs of the CT $\Delta\Sigma$ ADC versus process corner and supply voltage variations, under the temperature of 27 °C. It shows that the SQNRs of the CT $\Delta\Sigma$ ADC are between 77 and 84 dB with the five process corners and the supply voltage range from 0.95 to 1.25 V. The SQNR fluctuations across process corners are caused by the RC variations of the CT loop filter, which can be compensated via a factory calibration. Fig. 13(b) shows the simulated SQNRs of the CT $\Delta\Sigma$ ADC versus process corner and temperature variations, under the supply voltage of 1.1 V. It shows that all the simulated SQNRs are above 77 dB across the five process corners and the temperature range from −20 °C to 85 °C. The simulation results show the robustness of the proposed CT-DT hybrid architecture.

B. ELDC and Coefficient Scaling

In the idealistic architecture of Fig. 10, we have assumed the NS SAR quantizer to be delay free. In reality, the NS SAR quantizer delay can be a large portion of the sampling clock period and can degrade the overall $\Delta\Sigma$ ADC stability if uncompensated. The commonly used method for ELDC is to add a direct feedback path around the quantizer [33], which requires an additional DAC and an additional active adder. Thanks to the charge domain operation of the SAR ADC, the ELDC can be embedded inside the NS SAR quantizer [8], [9]. Comparing to the conventional ELDC method,

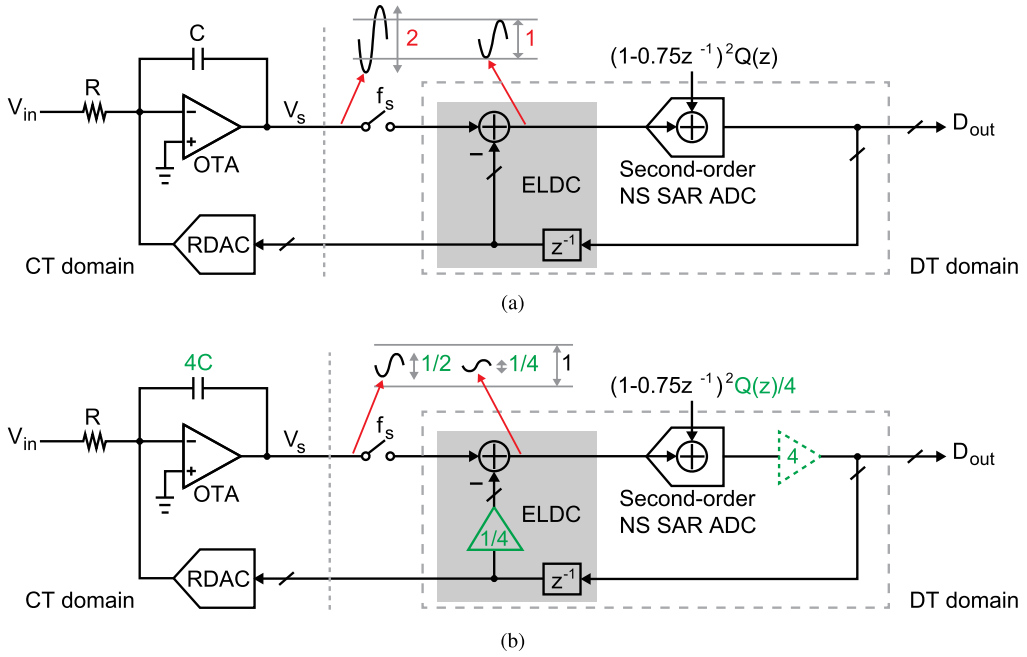


Fig. 14. Adapted models of proposed CT ΔΣ ADC with the second-order NS SAR quantizer and embedded ELDC (a) before and (b) after coefficient scaling.

the embedded charge domain ELDC obviates the need of the additional feedback DAC and adder, which reduces the circuit complexity, power, and area.

With the embedded charge domain ELDC, the model of the proposed ΔΣ ADC is adapted from Figs. 10 to 14(a). Yet, there is one more practical issue to address: the signal swing of the integrator output, V_s, becomes 2× of the full swing, resulting in saturation of the integrator. To address this issue, coefficient scaling is performed, as illustrated in Fig. 14(b). The ELDC component is attenuated by 1/4 before feeding back to the subtraction node. It is then recovered by a gain of 4 after NS SAR quantization. As will be shown later, the attenuation and the gain are realized by capacitor scaling, which does not require any active circuit. To maintain the loop gain of the overall ADC, the voltage gain of the CT loop filter is also attenuated by 1/4, which is achieved by scaling up the active integration capacitor by 4×. This way, the loop filter output swing becomes half of the full swing, thus avoiding saturation and improving the linearity of the integrator.

The price for the coefficient scaling is degraded noise suppression due to the reduced gain of the CT loop filter. After coefficient scaling, the amplitudes of the input referred kT/C noise and comparator noise are increased by 4×. The input referred quantization noise is unchanged because it is attenuated by 1/4 during the capacitor scaling. Nonetheless, because the kT/C noise is the first-order shaped and the comparator noise is third-order shaped, the degraded noise suppression is a minor issue compared to the benefits of removing active circuits for ELDC and improved integrator linearity.

C. Implementation of Proposed NS SAR Quantizer With ELDC

The ELDC and coefficient scaling are efficiently embedded in the NS SAR quantizer by adding a sub-DAC and an attenuation capacitor in the capacitor array, as shown in Fig. 15. The capacitor DAC (CDAC) for ELDC, C_{ELDC}, is a replica of the CDAC for SAR conversion, C_{SAR}. By adding an attenuation capacitor, C_{att}, the weight of C_{ELDC} is scaled down to 1/4 of the entire capacitor array, C_{DAC}. This realizes the coefficient of 1/4 for ELDC. At the same time, the weight of C_{SAR} is also scaled down to 1/4 of C_{DAC}. It reduces the quantization step size to 1/4 of that before the coefficient scaling, which is essentially equivalent to amplify the signal on C_{DAC} by 4×. The ELDC is performed in the sampling phase by feeding back the previous conversion results, $D_{3\sim0}[n-1]$, to the bottom plate of C_{ELDC}.

The bi-directional single-side DAC switching technique is used to suppress the comparator input common-mode variation and reduce the layout complexity [34], [35]. As the kT/C noise is small with the proposed NS SAR scheme, and it is the first-order shaped by the CT loop filter, small C_{DAC} size can be used to reduce DAC settling time and speed up the SAR conversion loop. In this design, the unit capacitor is 0.48 fF, C_{DAC} is 30 fF, C_1 and C_2 are 90 fF. Such a small unit capacitor size is realized by custom-designed metal-to-metal capacitor [36]. By careful layout, the unit capacitor mismatch can be made within 1%. The C_{DAC} mismatch error does not affect the overall ADC performance as it is high-pass filtered by the CT loop filter.

The detailed operation of the proposed NS SAR quantizer with ELDC is shown in Fig. 16(a). The comparator and logic circuits are not shown for simplicity purpose. In the sampling phase, the top plate of C_{DAC} is connected to the loop filter output, $V_s[n]$, while the bottom plate of C_{ELDC} is connected to the previous conversion results, $D_{3\sim0}[n-1]$, to realize the ELDC subtraction. The bottom plate of C_{SAR} is reset to "0111," which is the essential common mode but without using a dedicated V_{cm}. After sampling, the bottom plate of C_{ELDC} switches to "0111." The NS SAR conversion performs on

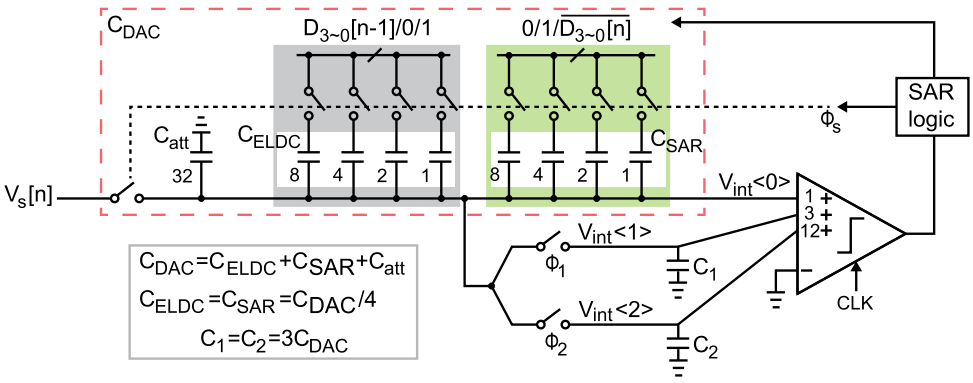


Fig. 15. Implementation of the proposed second-order NS SAR quantizer with embedded ELDC.

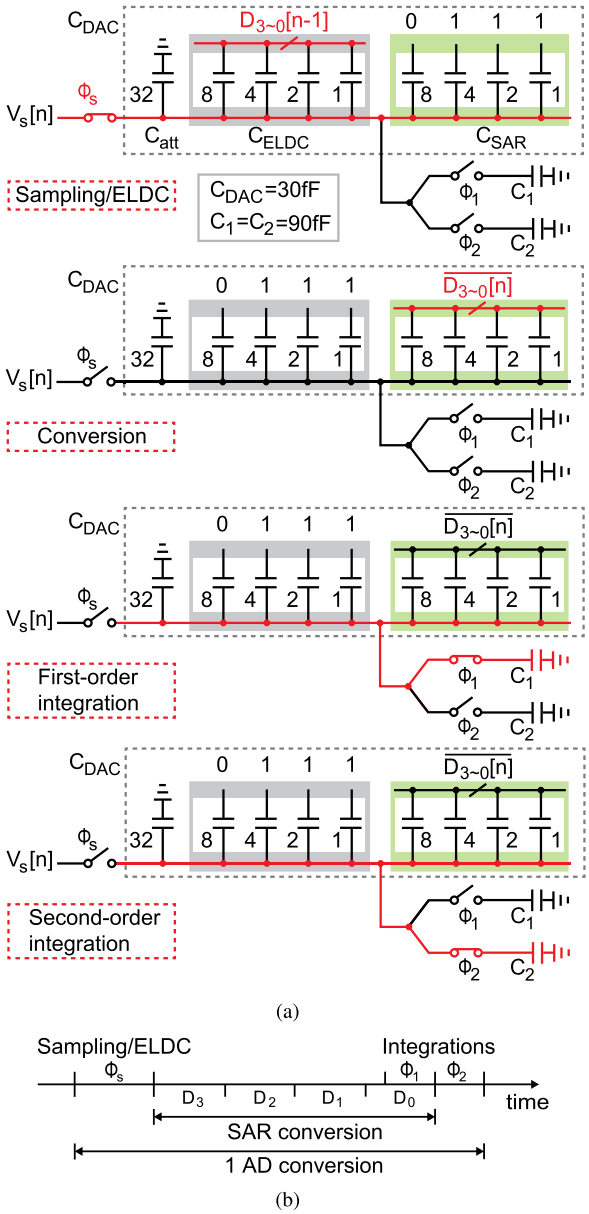


Fig. 16. (a) Operation and (b) timing of the NS SAR quantizer with ELDC.

C_{SAR} to resolve $D_{3\sim0}[n]$. At the end of the SAR conversion, C_{DAC} sequentially merges with C_1 and C_2 to perform the passive integrations. As the first-order passive integration can

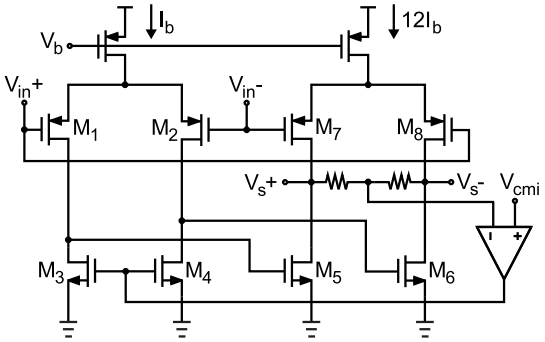


Fig. 17. Schematic of the OTA.

be absorbed in the last bit cycle of the SAR conversion, only six clock cycles are required for the entire operation including sampling/ELDC, 4-bit SAR conversion, and second-order integration, as shown in Fig. 16(b). Asynchronous clocking is used to speed up the operation and obviate the need for a high-frequency external clock [37].

D. OTA Design

A two-stage feedforward compensated OTA is employed in the *RC* integrator to achieve low power and wide bandwidth [38]. The schematic is shown in Fig. 17. Transistors M_{1-4} form the OTA's input stage. M_{5-6} form its output stage. The cascade of M_{1-4} and M_{5-6} provides a slow but high dc-gain path. Transistors M_{7-8} create a high-frequency feedforward path between the input and the output, thus stabilizing the OTA. M_{7-8} reuse the bias current of M_{5-6} to save power. To reduce the flicker noise, pMOS differential pairs are used. Based on the post-layout simulation, the OTA achieves 43-dB dc gain and 820-MHz unity-gain bandwidth (UGB), while consuming 0.45 mA from a 1.1-V supply.

E. RDAC Design

Fig. 18 shows the schematic of a unit cell of the 4-bit feedback DAC. Simple cross-coupled inverters with access transistors act as the retiming latch. RDAC is chosen over current source DAC for better matching and lower noise, especially under low supply voltage with limited overdrive voltage for the current source. A prior work [15] reports that an

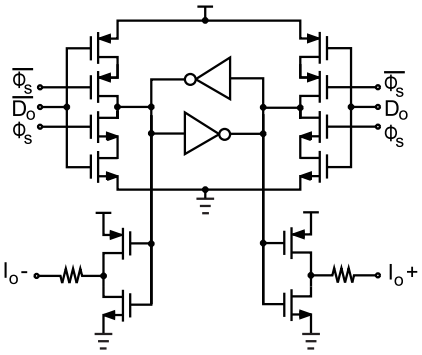


Fig. 18. Schematic of the RDAC unit cell.

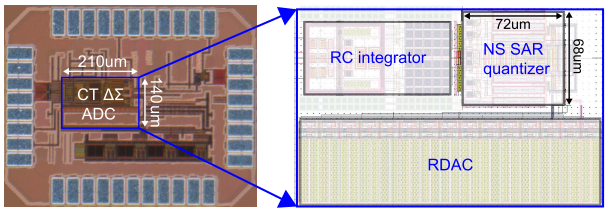


Fig. 19. Die photograph and layout.

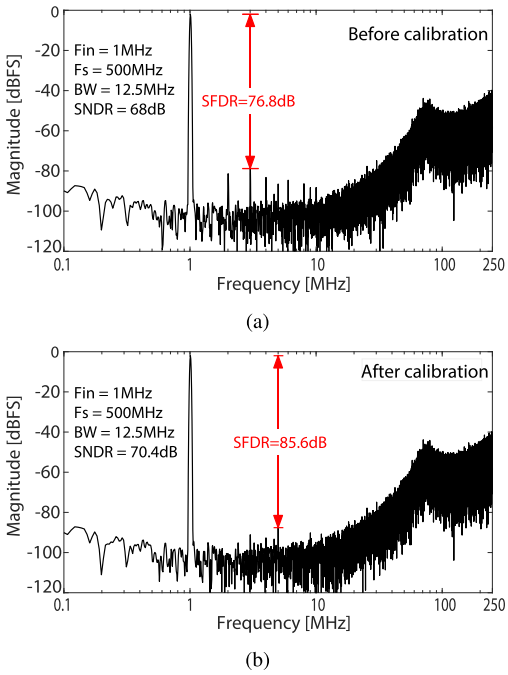


Fig. 20. Measured ADC output spectra (a) before and (b) after calibration.

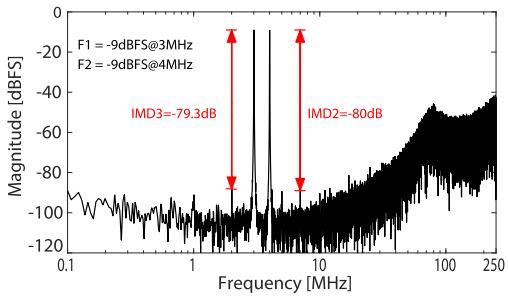


Fig. 21. Measured two-tone output spectrum.

RDAC can achieve nearly 2× better of matching than a current DAC, with the same layout area. In this design, RDAC with the large size (49 μm × 1 μm ×5) of unit resistor element is used to achieve a good raw matching. According to MC simulations, the standard deviation of mismatch between a unit resistor and the mean resistor value of RDAC array is only 0.1%. The main problem of an RDAC is that it adds resistive loading to the virtual ground of the *RC* integrator, resulting in increased OTA input referred noise and reduced loop gain, which need to be handled by appropriate overall power–noise tradeoffs. NRZ is chosen over return to zero to relax the requirement on clock jitter and loop filter linearity [33]. In this design, DEM is not applied in order to simplify the prototype ADC design. Instead, the off-chip foreground digital calibration is used to address the RDAC non-linearities. This calibration is performed by feeding in a sinusoidal test signal to excite all the bits, then applying the least squares regression to figure out the optimal element weights that yield the lowest harmonic distortion [37], [39]. The set of weights will then be frozen and applied to all subsequent measurements. The DAC mismatch error is the first-order PVT insensitive, ensuring robustness of the foreground calibration. However, the drawback of foreground calibration is that it suffers from long-term DAC error shifts, such as aging. Thus, periodically repeated calibrations may be required.

IV. Measurement Results

As a proof of concept, a prototype of the proposed third-order CT ΔΣ ADC with a second-order NS SAR quantizer is fabricated in a 40-nm CMOS process. Fig. 19 shows the die photograph and layout. The active area is 0.029 mm^2. Thanks to the significant capacitor size reduction described in Section II, the NS SAR quantizer occupies only 0.005 mm^2. The total on-chip decoupling is 14.9 pF. The breakdown is 3.4 pF for RDAC reference, 1.5 pF for CDAC reference, 1.5 pF for OTA supply, 2.3 pF for SAR analog supply, 2.4 pF for digital circuits, and 3.8 pF for output buffers.

Fig. 20 shows the measured output spectra with a 1-MHz input signal at the sampling frequency of 500 MHz. The measured SNDR is 68 dB in a 12.5-MHz bandwidth. The measured spurious-free dynamic range (SFDR) is 76.8 dB, limited by RDAC nonlinearity. After an off-chip foreground RDAC nonlinearity calibration, the measured SNDR, and SFDR are improved to 70.4 and 85.6 dB, respectively. The out-of-band peaking in the spectra is caused by increased delay in the RDAC feedback loop. In circuit designing, the loop delay of an entire sampling period ($1/f_s$) is set, which can be well compensated by our proposed ELDC. However, the parasitics in the feedback path cause considerably extra delay. The loop delay is estimated to be 1.2× of a sampling period according to our follow-up verifications.

Fig. 21 shows the measured spectrum with two input tones of −9 dBFS at 3 and 4 MHz. The measured second-order and third-order inter-modulation distortions (IMDs) are −80 and −79.3 dB, respectively.

Fig. 22 shows the measured SNDR and SNR versus the input amplitude. The peak SNDR and SNR are

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

Specifications	This work	ISSCC'13 Shu [3]	VLSI'15 Wei [8]	JSSC'16 Wu [9]	JSSC'18 Jang [10]	JSSC'16 Kim [12]	JSSC'17 Kim [20]	JSSC'14 Rao [17]	JSSC'17 Li [15]	ESSCIRC'16 Chen [21]
Quantizer	2nd-order NS SAR	Flash	SAR	SAR	SAR	NSIQ	DNSQ	VCO-based	VCO-based	1st-order NS SAR
Process [nm]	40	28	28	65	28	130	130	90	130	65
Area [mm^2]	0.029	0.08	0.066	0.16	0.1	0.08	0.17	0.16	0.13	0.097
Fs [MHz]	500	640	432	900	320	640	640	640	250	3.2
Bandwidth [MHz]	12.5	18	5	45	10	10	15	5	3	0.1
Peak SNDR [dB]	70.4	73.6	80.5	75.3	74.4	75.3	80.4	74.7	70.2	74.9
DR [dB]	73	78.1	83.9	82.5	80.8	78.5	82.9	77	77.6	78
Power [mW]	1.16	3.9	3.16	24.7	4.2	7.19	11.4	4.1	1.05	0.046
FoM_W [fJ/conv.-step]*	17.1	27.7	36.4	57.7	51	75.9	44.1	92	66.2	50
FoM_S [dB]**	170.7	170.2	172.5	167.9	168.1	169.9	171.6	165.6	164.8	168.3

*FoM_W = Power / (2× BW × $2^{(SNDR - 1.76)/6.02}$). **FoM_S = SNDR + $10\log_{10}$(BW / Power).

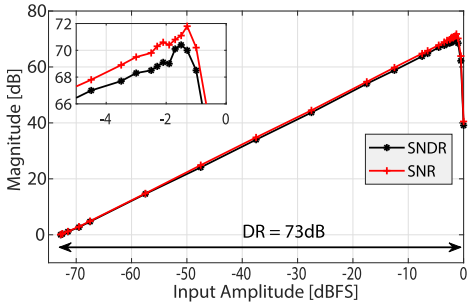


Fig. 22. Measured SNR and SNDR versus input amplitude.

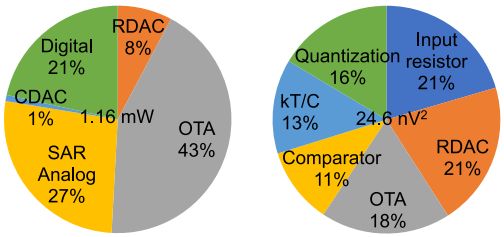


Fig. 23. (a) Measured power breakdown. (b) Calculated noise breakdown.

70.4 and 71.9 dB, respectively. The prototype ADC achieves 73 dB of dynamic range.

The prototype ADC consumes 1.16 mW of power, which does not include the power for off-chip reference generations and foreground RDAC calibration. The measured power breakdown is shown in Fig. 23(a). The OTA consumes the largest portion of 43%. The NS SAR analog supply, including the comparator and the bootstrap switches, consumes 27%. The digital supply, including the SAR logic and the DAC retiming latch, consumes 21%. The RDAC consumes 8%. The CDAC switching power is only 1%. The calculated in-band input referred noise breakdown is shown in Fig. 23(b). The total in-band noise is 24.6 nV^2. It translates to 72.4 dB of SNR with a −1.5-dBFS input, which matches well with the measurement result shown in Fig. 22. The input resistor and the RDAC contribute in total 42% of noise. The noise contributions of OTA, quantization error, kT/C, and comparator take up 18%, 16%, 13%, and 11%, respectively.

Table II summarizes the performance of the prototype ΔΣ ADC and compares it with the prior works. Overall, this paper achieves state-of-the-art performance. Owing to the compact and power-efficient architecture, it achieves the smallest active area of 0.029 mm^2 and the best Walden FoM of 17.1 fJ/conversion-step.

V. CONCLUSION

This paper presented a third-order hybrid CT-DT ΔΣ ADC with a single OTA and a fully passive second-order NS SAR quantizer. It combines the anti-alias filtering capability of CT ΔΣ ADC and the PVT robustness of the passive NS SAR ADC. Owing to the inherent second-order NS of the quantizer, the loop filter design is greatly simplified, the ADC power is reduced, and the overall robustness against *RC* product variation is improved. In addition, the proposed second-order NS SAR ADC achieves significant performance improvements upon the prior work. For the same thermal noise budget, it can reduce the total capacitor size by 2.4× and the comparator power by more than 40%. The proposed CT ΔΣ ADC is well suited for applications that demand low power, low design complexity, and high robustness.

ACKNOWLEDGMENT

The authors would like to thank Taiwan Semiconductor Manufacturing Company University Shuttle Program for chip fabrication.

REFERENCES

[1] S. Paton, A. D. Giandomenico, L. Hernandez, A. Wiesbauer, T. Potscher, and M. Clara, "A 70-mW 300-MHz CMOS continuous-time ΔΣ ADC with 15-MHz bandwidth and 11 bits of resolution," *IEEE J. of Solid-State Circuits*, vol. 39, no. 7, pp. 1056–1063, Jul. 2004.

[2] M. Bolatkale, L. J. Breems, R. Rutten, and K. A. A. Makinwa, "A 4 GHz continuous-time ΔΣ ADC with 70 dB DR and −74 dBFS THD in 125 MHz BW," *IEEE J. of Solid-State Circuits*, vol. 46, no. 12, pp. 2857–2868, Dec. 2011.

[3] Y. S. Shu, J. Y. Tsai, P. Chen, T. Y. Lo, and P. C. Chiu, "A 28fJ/conv-step CT ΔΣ modulator with 78dB DR and 18MHz BW in 28nm CMOS using a highly digital multibit quantizer," in *IEEE ISSCC Dig. Tech. papers*, Feb. 2013, pp. 268–269.

[4] M. Ranjbar, A. Mehrabi, O. Oliaei, and F. Carrez, "A 3.1 mW continuous-time $\Delta\Sigma$ modulator with 5-bit successive approximation quantizer for WCDMA," *IEEE J. of Solid-State Circuits*, vol. 45, no. 8, pp. 1479–1491, Aug. 2010.

[5] Z. Chen, Y. Jiang, C. Cai, H. G. Wei, S. W. Sin, U. Seng-Pan, Z. Wang, and R. P. Martins, "A 22.4μW 80dB SNDR $\Delta\Sigma$ modulator with passive analog adder and SAR quantizer for EMG application," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2012, pp. 257–260.

[6] H. C. Tsai, C. L. Lo, C. Y. Ho, and Y. H. Lin, "A 64-fJ/conv.-step continuous-time $\Delta\Sigma$ modulator in 40-nm CMOS using asynchronous SAR quantizer and digital $\Delta\Sigma$ truncator," *IEEE J. of Solid-State Circuits*, vol. 48, no. 11, pp. 2637–2648, Nov. 2013.

[7] C. Y. Ho, C. Liu, C. L. Lo, H. C. Tsai, T. C. Wang, and Y. H. Lin, "A 4.5 mW CT self-coupled $\Delta\Sigma$ modulator with 2.2 MHz BW and 90.4 dB SNDR using residual ELD compensation," *IEEE J. of Solid-State Circuits*, vol. 50, no. 12, pp. 2870–2879, Dec. 2015.

[8] G. Wei, P. Shettigar, F. Su, X. Yu, and T. Kwan, "A 13-ENOB, 5 MHz BW, 3.16 mW multi-bit continuous-time $\Delta\Sigma$ ADC in 28 nm CMOS with excess-loop-delay compensation embedded in SAR quantizer," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2015, pp. C292–C293.

[9] B. Wu, S. Zhu, B. Xu, and Y. Chiu, "A 24.7 mW 65 nm CMOS SAR-assisted CT $\Delta\Sigma$ modulator with second-order noise coupling achieving 45 MHz bandwidth and 75.3 dB SNDR," *IEEE J. of Solid-State Circuits*, vol. 51, no. 12, pp. 2893–2905, Dec. 2016.

[10] I. H. Jang, M. J. Seo, S. H. Cho, J. K. Lee, S. Y. Baek, S. Kwon, M. Choi, H. J. Ko, and S. T. Ryu, "A 4.2-mW 10-MHz BW 74.4-dB SNDR continuous-time $\Delta\Sigma$ modulator with SAR-assisted digital-domain noise coupling," *IEEE J. of Solid-State Circuits*, vol. 53, no. 4, pp. 1139–1148, Apr. 2018.

[11] N. Maghari and U. K. Moon, "A third-order DT $\Delta\Sigma$ modulator using noise-shaped bi-directional single-slope quantizer," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2882–2891, Dec. 2011.

[12] T. Kim, C. Han, and N. Maghari, "A 7.2 mW 75.3 dB SNDR 10 MHz BW CT $\Delta\Sigma$ modulator using Gm-C-based noise-shaped quantizer and digital integrator," *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1840–1850, Aug. 2016.

[13] M. Z. Straayer and M. H. Perrott, "A 12-bit, 10-MHz bandwidth, continuous-time $\Delta\Sigma$ ADC with a 5-bit, 950-MS/s VCO-based quantizer," *IEEE J. of Solid-State Circuits*, vol. 43, no. 4, pp. 805–814, Apr. 2008.

[14] K. Lee, Y. Yoon, and N. Sun, "A scaling-friendly low-power small-area $\Delta\Sigma$ ADC with VCO-based integrator and intrinsic mismatch shaping capability," *IEEE J. on Emerging and Selected Topics in Circuits and Syst.*, vol. 5, no. 4, pp. 561–573, Dec. 2015.

[15] S. Li, A. Mukherjee, and N. Sun, "A 174.3-dB FoM VCO-based CT $\Delta\Sigma$ modulator With a fully-digital phase extended quantizer and tri-level resistor DAC in 130-nm CMOS," *IEEE J. of Solid-State Circuits*, vol. 52, no. 7, pp. 1940–1952, Jul. 2017.

[16] M. Park and M. H. Perrott, "A 78 dB SNDR 87 mW 20 MHz bandwidth continuous-time $\Delta\Sigma$ ADC with VCO-based integrator and quantizer implemented in 0.13 μm CMOS," *IEEE J. of Solid-State Circuits*, vol. 44, no. 12, pp. 3344–3358, Dec. 2009.

[17] S. Rao, K. Reddy, B. Young, and P. K. Hanumolu, "A deterministic digital background calibration technique for VCO-based ADCs," *IEEE J. of Solid-State Circuits*, vol. 49, no. 4, pp. 950–960, Apr. 2014.

[18] G. Taylor and I. Galton, "A reconfigurable mostly-digital $\Delta\Sigma$ ADC with a worst case FOM of 160 dB," *IEEE J. of Solid-State Circuits*, vol. 48, no. 4, pp. 983–995, Apr. 2013.

[19] K. Ragab and N. Sun, "A 12-b ENOB 2.5-MHz BW VCO-based 0-1 MASH ADC with direct digital background calibration," *IEEE J. of Solid-State Circuits*, vol. 52, no. 2, pp. 433–447, Feb. 2017.

[20] T. Kim, C. Han, and N. Maghari, "A 4th-order continuous-time $\Delta\Sigma$ modulator using 6-bit double noise-shaped quantizer," *IEEE J. of Solid-State Circuits*, vol. 52, no. 12, pp. 3248–3261, Dec. 2017.

[21] Z. Chen, M. Miyahara, and A. Matsuzawa, "A stability-improved single-opamp third-order $\Delta\Sigma$ modulator by using a fully-passive noise-shaping SAR ADC and passive adder," in *Proc. European Solid State Circuits Conf. (ESSCIRC)*, Sep. 2016, pp. 249–252.

[22] W. Guo, H. Zhuang, and N. Sun, "A 13b-ENOB 173dB-FoM 2nd-order NS SAR ADC with passive integrators," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2017, pp. 236–237.

[23] J. Liu, S. Li, W. Guo, G. Wen, and N. Sun, "A 0.029mm^2 17fJ/Conv.-Step CT $\Delta\Sigma$ ADC with second-order noise-shaping SAR quantizer," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2018, pp. 201–202.

[24] J. A. Fredenburg and M. P. Flynn, "A 90-MS/s 11-MHz-bandwidth 62-dB SNDR noise-shaping SAR ADC," *IEEE J. of Solid-State Circuits*, vol. 47, no. 12, pp. 2898–2904, Dec. 2012.

[25] K. Obata, K. Matsukawa, T. Miki, Y. Tsukamoto, and K. Sushihara, "A 97.99 dB SNDR, 2 kHz BW, 37.1 μW noise-shaping SAR ADC with dynamic element matching and modulation dither effect," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2016, pp. 1–2.

[26] Y. S. Shu, L. T. Kuo, and T. Y. Lo, "An oversampling SAR ADC with DAC mismatch error shaping achieving 105 dB SFDR and 101 dB SNDR over 1 kHz BW in 55 nm CMOS," *IEEE J. of Solid-State Circuits*, vol. 51, no. 12, pp. 2928–2940, Dec. 2016.

[27] Z. Chen, M. Miyahara, and A. Matsuzawa, "A 9.35-ENOB, 14.8 fJ/conv.-step fully-passive noise-shaping SAR ADC," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2015, pp. C64–C65.

[28] W. Guo and N. Sun, "A 12b-ENOB 61 μW noise-shaping SAR ADC with a passive integrator," in *Proc. European Solid State Circuits Conf. (ESSCIRC)*, Sep. 2016, pp. 405–408.

[29] Z. Chen, M. Miyahara, and A. Matsuzawa, "A 2nd order fully-passive noise-shaping SAR ADC with embedded passive gain," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2016, pp. 309–312.

[30] C. C. Liu and M. C. Huang, "A 0.46mW 5MHz-BW 79.7dB-SNDR noise-shaping SAR ADC with dynamic-amplifier-based FIR-IIR filter," in *IEEE ISSCC Dig. Tech. papers*, Feb. 2017, pp. 466–467.

[31] S. Li, B. Qiao, M. Gandara, and N. Sun, "A 13-ENOB 2nd-order noise-shaping SAR ADC realizing optimized NTF zeros using an error-feedback structure," in *IEEE ISSCC Dig. Tech. papers*, Feb. 2018, pp. 234–236.

[32] R. J. Baker, "Sense amplifier design," in *CMOS: circuit design, layout, and simulation*. 3rd ed., Piscataway, New Jersey, USA: Wiley-IEEE Press, 2010, ch. 16, sec. 2, pp. 448–456.

[33] S. Pavan, R. Schreier, and G. C. Temes, "Feedback DAC design," in *Understanding Delta-Sigma Data Converters*. 2nd ed., Piscataway, New Jersey, USA: Wiley-IEEE Press, 2017, ch. 10, sec. 7, pp. 320–331.

[34] A. Sanyal and N. Sun, "An energy-efficient low frequency-dependence switching technique for SAR ADCs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 5, pp. 294–298, May 2014.

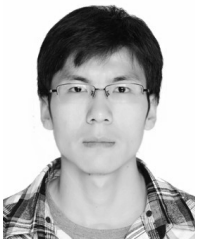
[35] L. Chen, K. Ragab, X. Tang, J. Song, A. Sanyal, and N. Sun, "A 0.95-mW 6-b 700-MS/s single-channel loop-unrolled SAR ADC in 40-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 3, pp. 244–248, Mar. 2017.

[36] P. J. A. Harpe, C. Zhou, Y. Bi, N. P. van der Meijs, X. Wang, K. Philips, G. Dolmans, and H. de Groot, "A 26 μW 8 bit 10 MS/s asynchronous SAR ADC for low energy radios," *IEEE J. of Solid-State Circuits*, vol. 46, no. 7, pp. 1585–1595, Jul. 2011.

[37] S. W. M. Chen and R. W. Brodersen, "A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13-μm CMOS," *IEEE J. of Solid-State Circuits*, vol. 41, no. 12, pp. 2669–2680, Dec. 2006.

[38] L. J. Breems, R. Rutten, R. H. M. v. Veldhoven, and G. v. d. Weide, "A 56 mW continuous-time quadrature cascaded $\Sigma\Delta$ modulator with 77 dB DR in a near zero-IF 20 MHz band," *IEEE J. of Solid-State Circuits*, vol. 42, no. 12, pp. 2696–2705, Dec. 2007.

[39] H. Garvik, C. Wulff, and T. Ytterdal, "An 11.0 bit ENOB, 9.8 fJ/conv.-step noise-shaping SAR ADC calibrated by least squares estimation," in *2017 IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2017, pp. 1–4.



Jiaxin Liu (S'13) received the B.S. degree from Shandong University, Jinan, China, in 2010, and the M.S. and Ph.D. degrees from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2013 and 2018, respectively.

From 2015 to 2017, he was a Visiting Ph.D. Student with the Department of Electrical and Computer Engineering, The University of Texas (UT) at Austin, Austin, TX, USA. He is currently a Post-Doctoral Researcher with Tsinghua University, Beijing, China. His current research interest is on the power-efficient data converters, especially on the topics of SAR-based hybrid ADCs, predicting ADCs and mismatch error shaping techniques. His broad research interests include RF, analog and mixed-signal integrated circuits design.

Dr. Liu was a recipient of the First Prize of Academic Scholarship in UESTC for the consecutive years from 2012 to 2015, the China National Scholarship in 2012, the First Prize of VeriSilicon Circuits Design Competition in 2015, and the China CSC Scholarship in 2015.

Shaolan Li (S'12) received the B.Eng. degree (Hons.) from The Hong Kong University of Science and Technology (HKUST), Hong Kong, in 2012, and the Ph.D. degree from The University of Texas at Austin, Austin, TX, USA, in 2018.

From 2013 to 2014, he held intern positions at Broadcom Ltd., Sunnyvale, CA, USA, and NXP Semiconductor, Tempe, AZ, USA. He is currently a Post-Doctoral Researcher with The University of Texas (UT) at Austin, Austin, TX, USA. His current research interests include low-power data converters, synthesizable mixed-signal circuits, and sensor interfaces.

Dr. Li was a recipient of the Academic Achievement Medal from HKUST in 2012, the HKUST Undergraduate Scholarship from 2010 to 2012, the UT Austin Cockrell School of Engineering Fellowship in 2017, and the IEEE SSCS Pre-Doctoral Achievement Award from 2017 to 2018. He serves as a reviewer for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-I (TCAS-I) and the IEEE TCAS-II.

Wenjuan Guo (S'13–M'17) received the B.S. degree from the Institute of Microelectronics and Nanoelectronics, Tsinghua University, Beijing, China, in 2011, and the Ph.D. degree from The University of Texas at Austin, Austin, TX, USA, in 2016.

She is currently an Analog Engineer with Intel Corporation, Austin, TX, USA. From 2013 to 2014, she was a Design Co-Op with Texas Instruments at Dallas, Dallas, TX, USA. Her current research is focused on analog and mixed-signal integrated circuits design.

Dr. Guo was a recipient of the Texas Instruments Ph.D. Fellowship in 2014 and 2015.

Guangjun Wen (M'04–SM'10) received the B.S. and M.E. degrees from Chongqing University, Chongqing, China, in 1986 and 1992, respectively, and the Ph.D. degree from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 1998.

From 1986 to Feb. 1995, he was a Lecturer with Chongqing University. He was with UESTC, from 1998 to 2000, and then with the Electronics and Telecommunication Research Institute, South Korea, from 2000 to 2001, as a Post-Doctoral Fellow. From 2001 to 2002, he was a Research Fellow with Nanyang Technological University, Singapore. From 2002 to 2005, he was a Senior RF Design Engineer with VS Electronic Pte. Ltd, Singapore, and the Sumitomo Electric Group, Yokohama, Japan. Since2004, he has been a Full Professor with UESTC. He has authored or co-authored more than 200 journal papers and presented more than 120 conference papers. His research interests are in radio frequency integrated circuits and systems for various wireless communication systems, RFID tag and reader, and circuit components and antennas design for the Internet of Things.

Nan Sun (S'06–M'11–SM'16) received the B.S. degree (Hons.) from the Department of Electronic Engineering, Tsinghua University, Beijing, China, in 2006, and the Ph.D. degree from the School of Engineering and Applied Sciences, Harvard University, Cambridge, MA, USA, in 2010.

He is currently an Associate Professor with the Department of Electrical and Computer Engineering, The University of Texas (UT) at Austin, Austin, TX, USA. His current research interests include analog, mixed-signal, and RF integrated circuits; miniature spin resonance systems; magnetic sensors and image sensors; micro- and nano-scale solid-state platforms (silicon ICs and beyond) to analyze biological systems for biotechnology and medicine.

Dr. Sun holds the AMD Endowed Development Chair from 2013 to 2017. He was a recipient of the NSF Career Award in 2013 and the Jack Kilby Research Award from UT Austin in both 2015 and 2016. He serves on the Technical Program Committee of the IEEE Custom Integrated Circuits Conference and the IEEE Asian Solid-State Circuit Conference. He is an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-I: REGULAR PAPERS and a Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS.