A 0.029mm^2 17-fJ/Conv.-Step CT $\Delta\Sigma$ ADC With 2nd-Order Noise-Shaping SAR Quantizer

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Abstract

This paper presents a compact and power-efficient 3rd-order CT $\Delta\Sigma$ ADC with a single OTA. A 4-b fully-passive 2nd-order noise-shaping SAR ADC is employed as the quantizer that inherently provides two additional noise shaping orders. Fabricated in 40nm CMOS, the prototype ADC consumes 1.16mW with a 500MHz clock rate. It achieves a Walden FoM of 17-fJ/conv.-step and occupies an area of only 0.029 mm^2.

Introduction

The emerging efforts on noise-shaping (NS) quantizers [1]–[4] provide attractive solutions for low-power and wideband $\Delta\Sigma$ modulators (DSMs). The noise-shaped integrating quantizer (NSIQ) of [1] achieves 1st-order NS but it suffers from a tradeoff between the speed and quantizer resolution. The double noise-shaped quantizer (DNSQ) of [2] achieves 2nd-order NS and 6-bit resolution by incorporating two quantizers. Yet, the leakage and gain mismatch from both quantizers degrade the overall performance. Voltage controlled oscillator (VCO) based quantizer has inherent 1st-order NS capability [3], but is often nonlinear and sensitive to PVT variation. In [4], a fully passive 1st-order NS SAR quantizer is proposed. However, its NS capability is limited and the overall DSM transfer function is still sensitive to PVT variation.

This paper presents a 3rd-order continuous-time (CT) DSM with a 2nd-order NS SAR quantizer. The proposed NS SAR quantizer has several key advantages compared to prior NS quantizers. First, its circuit is simple. It requires only a few extra switches, capacitors, and comparator input pairs on top of a classic SAR. Second, it is OTA-free and highly scaling friendly. Third, the quantizer noise transfer function (NTF) is set by component ratios, thus is highly robust against PVT variation. Last, it greatly simplifies the excess loop delay compensation (ELDC) by embedding it in the SAR. Owing to the inherent 2nd-order noise shaping of the quantizer, the loop filter is simplified to have only a single OTA. The ADC power is reduced and the overall loop stability is improved.

Proposed CT DSM with 2nd-order NS SAR Quantizer

Fig. 1 shows the architecture of the proposed 3rd-order CT DSM, which consists of a 1st-order CT loop filter and a new 2nd-order NS SAR quantizer with ELDC. The CT loop filter contains a feedforward-compensated OTA-based RC integrator and a 4-bit non-return-to-zero (NRZ) resistive DAC (RDAC). The ELDC is embedded in the capacitive DAC (CDAC) of the NS asynchronous SAR (ASAR) quantizer, whose circuit implementation is shown in Fig. 2. The ELDC leverages charge sharing and reference scaling to implement summation and gain without needing OTA. During sampling, the digital output in the previous cycle, $D[n-1]$, is subtracted from the input through ELDC CDAC while SAR CDAC is reset. After sampling, ELDC CDAC is reset and then the SAR conversion starts. The attenuation capacitor C_{att} is used to scale down the reference voltage of SAR and ELDC by a factor of $a = 4$. This recovers the loop gain of the DSM. In addition, it reduces the loop filter output swing by 2 times, thus improves the linearity of the OTA-based integrator. In this design, the total input capacitance of the NS SAR quantizer, C_{DAC}, is 30fF.

The proposed 2nd-order NS SAR is realized with only two switches, two capacitors and two extra comparator input pairs on top of a classic SAR. After the normal SAR operation, the residue voltage on the CDAC is integrated with two capacitors C_1 and C_2 sequentially. As the first integration cycle for S_1 can be absorbed in the last bit of SAR conversion, only one extra clock cycle for S_2 is required. The NTF zeros of the NS SAR are determined by the ratios of C_{DAC} to C_1 and C_2. In this design, both C_1 and C_2 are 90fF, the NTF zeros are set at $b = 0.75$ to balance the trade-off between noise-shaping effect and signal attenuation during the passive integration. A 3-input-pair dynamic comparator works as the adder in the feedforward path. The three input pairs are sized with the ratio of 1:3:12 to provide the gains (g_1 and g_2) to compensate for the signal attenuation during passive integration.

The proposed 2nd-order NS SAR has several advantages over the prior design of [5]. As shown in Fig. 3, the prior work uses a small capacitor C_0 to sample the CDAC residue voltage. By contrast, the proposed scheme obviates the need for C_0; instead, it directly connects C_{DAC} to C_1 and C_2 for integration. This approach brings two key merits. First, it removes the large kT/C noise due to the sampling operation on the small C_0. For the same overall kT/C noise budget, the proposed NS SAR can reduce the total capacitor size by 2.4 times, leading to a significant area reduction. The 5-time reduction in C_{DAC} also accelerates the SAR operation speed by shortening the DAC settling time. Second, it avoids the signal attenuation of 3/4 due to the sampling on C_0. This relaxes the comparator noise requirement. It also reduces the comparator input pair ratio from 1:4:16 of [5] to 1:3:12. For the same comparator input referred noise budget, the proposed scheme reduces the comparator power by more than 40%.

Fig. 4 shows the schematic of the dynamic comparator in the NS SAR quantizer. A 3-stage architecture is used to achieve high speed and low noise. The relative gain between the 3 input paths is realized by sizing the input-pair widths differently. The input pairs are clocked through their drains and grounded through the sources, which reduces the kick-back noise by 2 times. Two inverters form the middle stage, which provides extra gain to accelerate the pre-amplification phase and reduce the noise from the last latch stage.

Measurement results

A prototype CT DSM is fabricated using 40nm CMOS process. Fig. 5 shows the die photo and layout, the active area is 0.029mm^2 while the NS SAR quantizer occupies only 0.005mm^2. Clocked at 500MHz, the modulator consumes

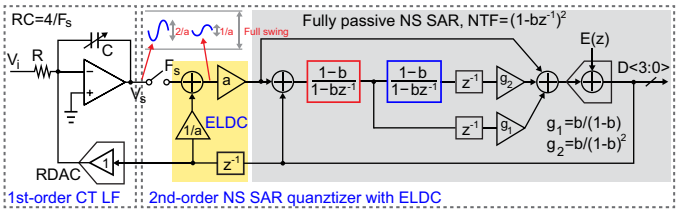


Fig. 1 Proposed CT DSM architecture.

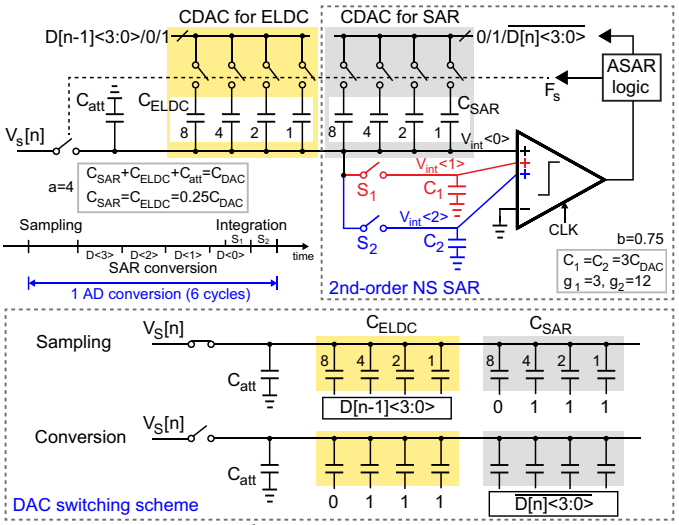
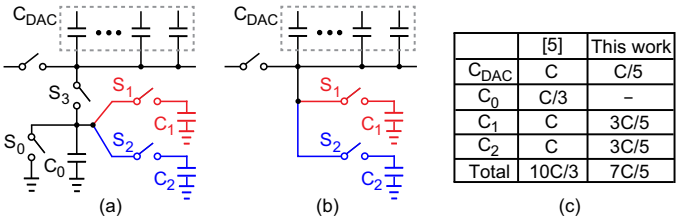


Fig. 2 Proposed 2nd-order NS SAR quantizer with ELDC.



	[5]	This work
C_{DAC}	C	C/5
C_0	C/3	–
C_1	C	3C/5
C_2	C	3C/5
Total	10C/3	7C/5

Fig. 3 (a) Prior NS SAR scheme of [5]; (b) Proposed NS SAR scheme. (c) Capacitor values for the same overall kT/C noise.

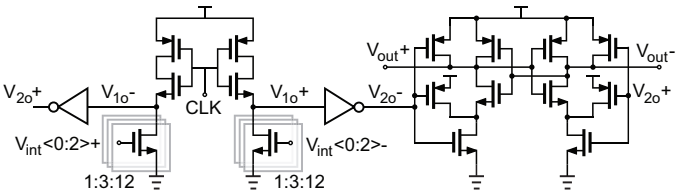


Fig. 4 Schematic of the proposed 3-stage 3-input-pair comparator.

1.16mW. The power breakdown is 0.5mW for OTA, 0.09mW for RDAC and 0.57mW for the quantizer. Fig. 6 shows the measured output spectra with 1MHz input signal. Before the DAC non-linearity calibration, the modulator achieves 68dB SNDR and 76.8dB SFDR over 12.5MHz bandwidth. After calibration, the SNDR and SFDR are improved to 70.4dB and 85.6dB, respectively. With two in-band tones of −9dBFS at 3MHz and 4MHz, the measured IMD2 and IMD3 are −80dB and −79.3dB, respectively. Fig. 7 shows the measured dynamic range, the peak SNDR and the peak SNR are 73dB, 70.4dB and 71.9dB, respectively. Table I summarizes the performance and compares it with prior works. This work represents the state-of-the-art performance for DSMs using NS quantizers, with strong highlights in its small chip area and high power efficiency.

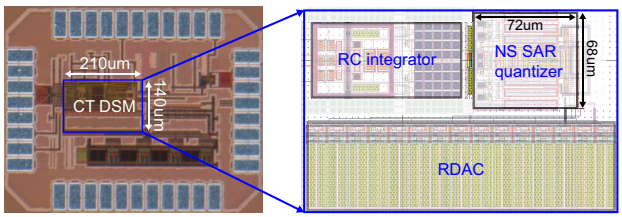


Fig. 5 Die photo and layout.

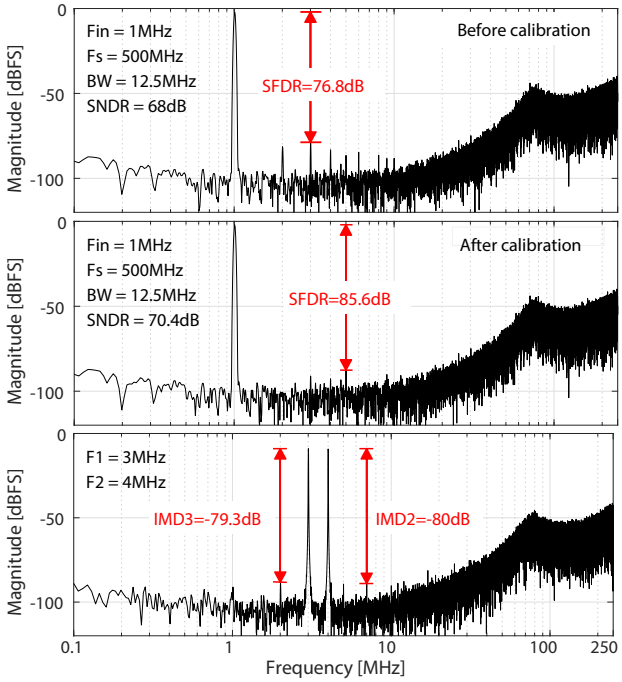


Fig. 6 Measured output spectrum.

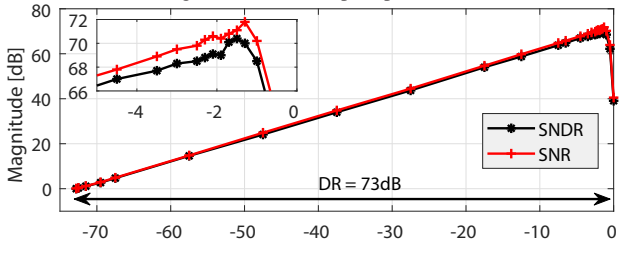


Fig. 7 Measured SNR/SNDR vs input amplitude.

TABLE I Performance comparision.

Specifications	**This work**	[2]	[3]	[4]	[6]
Quantizer	**2nd-order NS SAR**	DNSQ	VCO-based	1st-order NS SAR	SAR
Process [nm]	**40**	130	90	65	65
Area [mm²]	**0.029**	0.17	0.16	0.097	0.16
Fs [MHz]	**500**	640	640	3.2	900
OSR	**20**	21.3	64	16	10
BW [MHz]	**12.5**	15	5	0.1	45
SNDR [dB]	**70.4**	80.4	74.7	74.9	75.3
Power [mW]	**1.16**	11.4	4.1	0.046	24.7
FoM_W [fJ/conv.-step]	**17.1**	44.1	92	50	57.7

FoM_W=Power/(2·BW·2^((SNDR-1.76)/6.02)).

References

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