16.5 A 13b 0.005mm² 40MS/s SAR ADC with kT/C Noise Cancellation

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As with any ADC with a front-end S/H, the SAR ADC suffers from a fundamental SNR challenge: its sampling kT/C noise. To satisfy the SNR requirement, the input capacitor has to be sufficiently large (e.g. 3pF for a 13b ADC with $2V_{pp}$ swing). This, however, makes it very costly to design the ADC input driver and the reference buffer. The input driver and the reference buffer are the bottleneck nowadays. Their power, area, and design complexity can be an order of magnitude higher than the SAR ADC core.

Since the root of the problem is the large input capacitor, it is highly desirable to figure out ways to reduce its size without incurring a kT/C noise penalty. In [1] a source follower is placed before the CDAC to prevent it from loading the ADC input, but this only shifts the burden to the source follower, which still needs to drive large sampling capacitors (7pF) limited by the kT/C noise. The source follower consumes extra current and produces extra noise, which degrades the overall ADC power efficiency. In [2] a 2-step ADC with a 1st-stage continuous-time (CT) SAR that is free from kT/C noise is proposed. It permits the use of a small differential input capacitor of only 120fF. Nevertheless, it suffers from several limitations: 1) the input signal frequency is limited to only 1MHz to prevent large tracking errors from the CT-SAR; 2) each CT SAR cycle is only 500ps. Even though the capacitor size is reduced, ensuring settling within such a short time remains a challenge for the ADC driver and the reference buffer; 3) it cannot convert a DC signal. These issues limit its application space.

This paper presents a 13b 40MS/s SAR ADC with a kT/C noise-cancellation technique. It enables substantial capacitor size reduction, and is free from the limitations of [1-2]. Figure 16.5.1 shows the architecture. Comparing to the conventional SAR with bottom-plate sampling and a comparator preamp, the only additional circuits are a capacitor C_2 and a switch, placed in between the comparator preamp and latch. In the noise-cancelling SAR, although C_1 appears as the sampling capacitor, the real sampling happens at C_2. When ϕ_1 turns off, the input switch connecting to V_{in} is still on, and thus, V_{in} is still being tracked by C_2 at the preamp output. The real sampling moment is the falling edge of ϕ_2. The role of C_1 is not to sample V_{in}, but to keep a low signal swing at the preamp input, so that the preamp does not saturate during Δt (i.e., the time difference between falling edges of ϕ_1 and ϕ_2.) When ϕ_1 turns off, there is a sampling kT/C_1 noise across C_1, but it is frozen on C_1 and acts just like an offset at preamp input. It is amplified and stored across C_2. Since C_2 works in the output series offset cancellation configuration, the kT/C_1 noise is canceled at the right side of C_2 [3]. When ϕ_2 turns off, the kT/C_2 noise is introduced on C_2, but since it is after the preamp, its input referred noise is greatly suppressed by the preamp gain A. Hence, C_1 and C_2 can be reduced to only 120fF and 50fF in this work but without causing large kT/C noise. The significant reduction in capacitor sizes can lead to substantial power and area savings for the ADC input driver and the reference buffer.

Figure 16.5.2 shows the detailed operation. When ϕ_1 is on, V_{in} is tracked on C_1. The preamp offset v_{os} is amplified and stored on C_2. At the falling edge of ϕ_1, C_1 stores both the sampled input $V_{in}(t_1)$ and the kT/C_1 noise v_{ns1}. When ϕ_1 turns off, ϕ_2 is still on. Thus, V_{in} is still tracked by C_2 after the preamp. The real sampling happens at the falling edge of ϕ_2. When ϕ_2 turns off, C_2 stores the amplified version of the sampled input $V_{in}(t_2)$ subtracted by C_1 voltage $V_{in}(t_1)+v_{ns1}$ and the offset v_{os}, together with the kT/C_2 noise v_{ns2}. During the SAR conversion phase, the digital codes are fed to the bottom plate of the CDAC (i.e., left of C_1), and the SAR logic attempts to bring the right side of C_2 to zero. Thus, ignoring other circuit non-idealities, we can derive that $D_{out}=V_{in}(t_2)+v_{ns2}/A$. The kT/C_1 noise v_{ns1} is cancelled and does not show up in D_{out}. Thus, theoretically speaking, C_1 can be made arbitrarily small but without incurring large kT/C_1 noise penalty. The kT/C_2 noise v_{ns2} is suppressed, and thus, permitting the use of a small C_2. Note that the preamp offset $_{Vos}$ is also cancelled. Thus, the kT/C noise cancellation technique also lowers the ADC offset and the flicker noise. $V_{in}(t_1)$ does not show up in D_{out}. As mentioned earlier, the role of C_1 sampling is only to keep a small signal swing at the preamp input, so that the preamp does not saturate during input tracking. The final ADC output D_{out} corresponds to V_{in} sampled at t_2.

For ease of explanation, the analysis so far has assumed the preamp fully settles during Δt. In reality, Δt needs to be kept short (0.6 ns in this design) to minimize the input variation $V_{in}(t_2)$-$V_{in}(t_1)$ and prevent the preamp from saturation during Δt. With a finite bandwidth, the preamp does not fully settle. The residual noise due to preamp incomplete settling can be calculated to be $kT/C_1 \cdot e^{-2\Delta t/\tau}$, where τ is the preamp settling time constant [3]. Thus, even though the kT/C_1 noise is not completely cancelled, it decreases very rapidly with $\Delta t/\tau$. In this design, the number of time constants allocated for preamp settling is only 2 (τ=0.3ns), but this is already sufficient to cancel 98% of the kT/C_1 noise (i.e., 50 times reduction).

Figure 16.5.3 shows the detailed circuit implementation of the prototype 13b SAR ADC. Since C_1 is only 120fF, it adopts a bridge capacitor topology to keep a reasonable unit capacitor size of 0.85fF. Three redundant capacitors are added to tolerate intermediate conversion errors. The comparator preamp is a single-stage common-source amplifier with the gain A of 6. It adopts a CMOS input stage to double the current efficiency. A load capacitor C_L of 100fF is added at the preamp output to limit its bandwidth during the SAR conversion phase and reduce the total comparator noise. A slight difference between Fig. 16.5.3 and Fig. 16.5.1 is that the ϕ_1 switch connects the preamp input not to an AC ground, but to the preamp output. This way, a large portion of the preamp offset v_{os}, is cancelled directly at the preamp input, which helps lower the preamp output signal swing.

The prototype SAR is fabricated in a 40nm CMOS process. The total power consumption is 591μW, where the breakdown is 28μW for the DAC, 280μW for the comparator preamp, 75μW for the comparator latch and bootstrap switches, and 208μW for the digital circuits. Figure 16.5.4 shows the measured output spectra with low-frequency (1.01MHz) and high-frequency (19.1MHz) full-swing ($2.2V_{pp}$) input signals. Foreground calibration is used to address the CDAC mismatches. Figure 16.5.5 shows the measured SNDR and SFDR with input frequency and amplitude sweeps. It ensures an SNDR of 69dB and an SFDR of 79dB across the entire Nyquist band. The measured dynamic range is 72dB.

Figure 16.5.6 summarizes the performance and compares it with prior works. Owing to the significant capacitor reduction from the noise-cancelling technique, it has the smallest chip area of only 0.005mm² among published state-of-the-art Nyquist ADCs with ≥11b ENOB [4]. Compared with prior kT/C noise-reduction techniques [2], this work supports DC and expands the signal bandwidth by 20 times. It also obviates the need for fast input/reference buffer settling. Compared to [1], which also lowers the input capacitance, this work eliminates the need for the large internal sampling capacitor of 7pF. Additionally, it improves the power efficiency by over 40 times. Compared with other state-of-the-art ADCs [5]–[7], this work achieves comparable performance. More importantly, it reduces the differential input capacitance by over 15 times, which will lead to significant power and area savings on the system level when considering the ADC input driver and reference buffer as a whole.

Acknowledgements:
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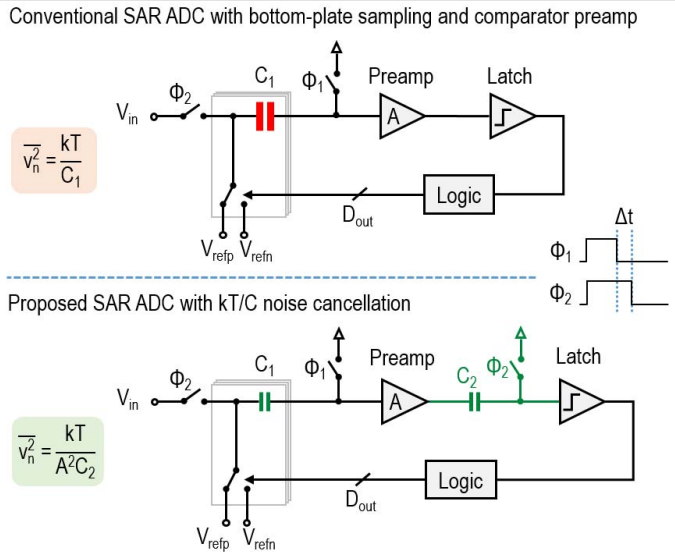

Figure 16.5.1: Principle of the proposed SAR ADC with kT/C noise cancellation.

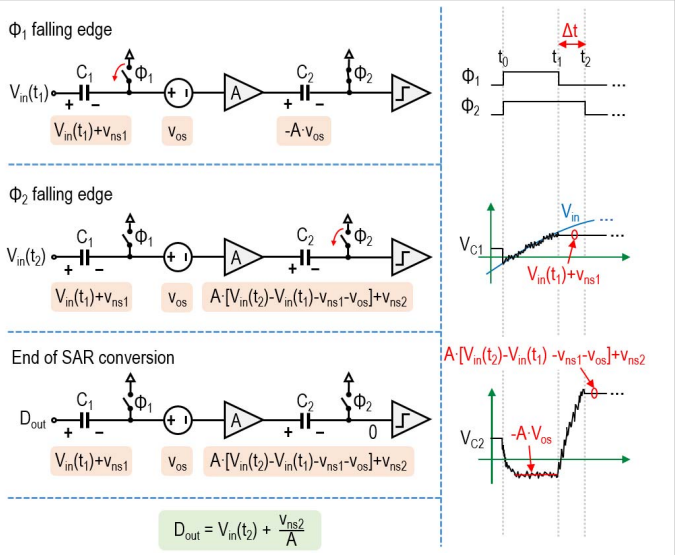

Figure 16.5.2: Operation of the proposed SAR ADC with kT/C noise cancellation.

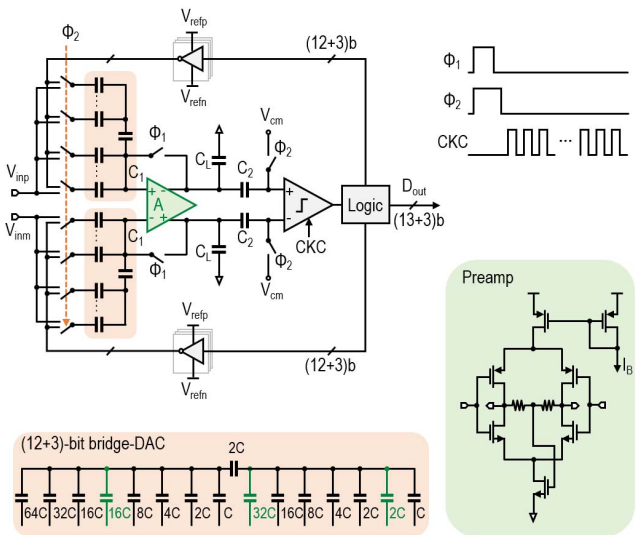

Figure 16.5.3: Circuit implementation of a 13b SAR ADC with kT/C noise cancellation.

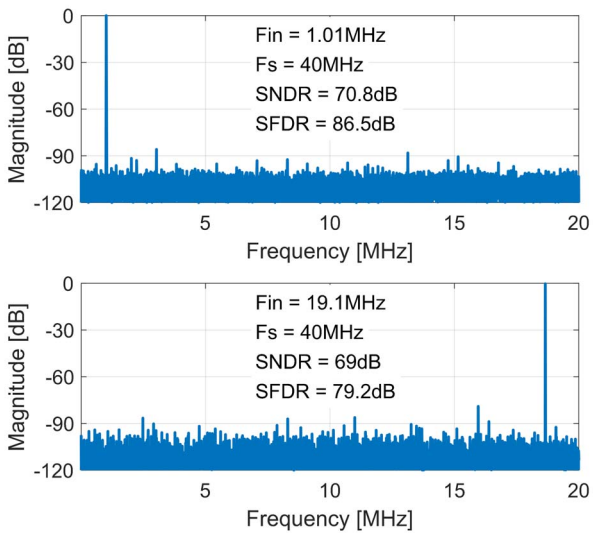

Figure 16.5.4: Measured output spectra with low-frequency and high-frequency input signals.

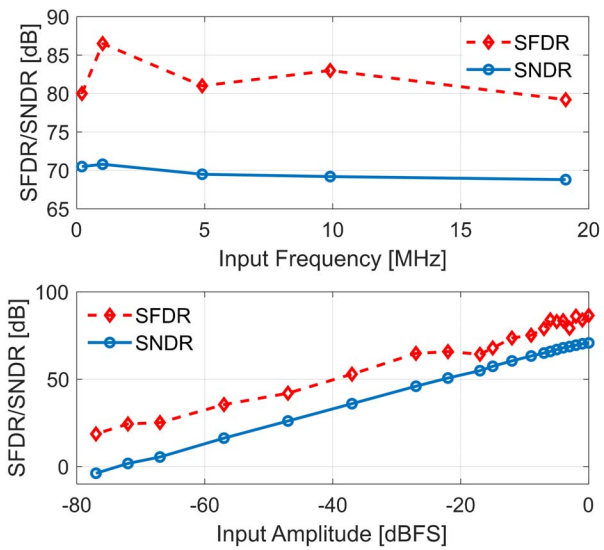

Figure 16.5.5: Measured SFDR/SNDR versus input frequency and amplitude.

	This work	ISSCC 2019 [2]	ISSCC 2015 [1]	JSSC 2017 [5]	ISSCC 2015 [6]	ISSCC 2013 [7]
Technology	**40nm**	40nm	40nm	40nm	65nm	65nm
Architecture	**SAR**	CT 2-step SAR	SAR	SAR	Pipe-SAR	SAR
kT/C Noise Suppressed?	**√**	√	×	×	×	×
Applicable for DC Signal?	**√**	×	√	√	√	√
Applicable for HF Signal?	**√**	×	√	√	√	√
Without the Need for Fast Input/Ref. Buf. Settling?	**√**	×	√	√	√	√
ADC Input Cap. (pF)	**0.24**	0.12	0.4	16	4	8.2
Internal Sampling Cap. (pF)	**0.3**	0.3	7	-	0.67	-
Area (mm^2)	**0.005**	0.01	0.236	0.32	0.054	0.55
Resolution (bits)	**13**	13	14	15	13	14
Sampling Rate (MS/s)	**40**	2	35	0.02	50	80
$SFDR_{NYQ}$ (dB)	**79.2**	79.4	90	95.1	84.6	80.3
$SNDR_{NYQ}$ (dB)	**69**	71.7	74.4	74.1	70.9	71.3
Power (uW)	**591**	25	42500	1.17	1000	31100
FoMs (dB)	**174.3**	177.8	160.6	173.4	174.9	164.7
FoMw (fJ/conv-step)	**6.4**	3.9	283	14.1	6.9	129

Figure 16.5.6: Performance summary and comparison.

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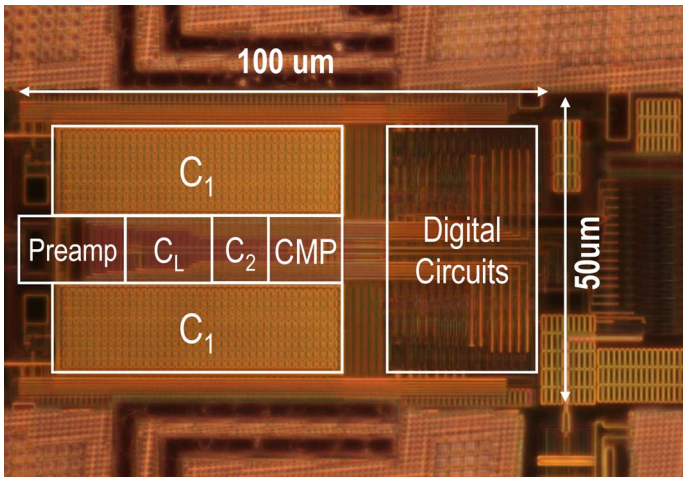

Figure 16.5.7: Die micrograph.

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