

9.3 A 40kHz-BW 90dB-SNDR Noise-Shaping SAR with 4× Passive Gain and 2nd-Order Mismatch Error Shaping

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Noise-shaping (NS) SAR ADCs using passive loop filters have drawn increasing attention due to their simplicity, low power, zero static current, and PVT robustness. However, prior works show limited resolution ($\text{ENOB} \leq 13\text{b}$) due to two main challenges. The 1st one is thermal noise. Passive loop filters cannot provide gain [1]. Hence, their suppression of the comparator noise is limited. In addition, every capacitor switching introduces extra kT/C noise. To reduce noise, a passive gain of 2 is realized in [2]. It also realizes passive voltage summation, which obviates the need for a multipath comparator, further reducing the comparator noise. Nevertheless, it uses small capacitors for residue sampling to minimize signal attenuation, leading to a large total kT/C noise of $20kT/C$ (C is the DAC size). Also, its NTF is mild (zero at 0.5), leading to limited SQNR benefit. The 2nd challenge is DAC mismatch. Classic DEM is unsuitable for SARs with a high-resolution DAC due to excessive hardware cost. To reduce circuit complexity, Ref. [3] applies DEM only to the MSB part of the DAC, but the LSB part still produces considerable errors. The mismatch error shaping (MES) technique of [4] is well suited for high-resolution binary DACs due to low hardware complexity, but it has its own limitations. First, it can only achieve 1st-order shaping with limited error suppression capability. Also, being 1st-order, it has strong signal dependence and can produce considerable tones, especially at low input amplitudes. In addition, it suffers from signal range loss.

This paper presents a 90dB-SNDR passive NS SAR that addresses the above challenges. It has an efficient architecture that realizes 4× passive gain and an NTF with zero at 0.8. It also removes the residue sampling, reducing the total kT/C noise. Compared with [2], it reduces the comparator power by 2.8× and the total kT/C noise power by 5.5×, and its NTF achieves 4.4dB SQNR gain. Moreover, it realizes 2nd-order MES that is tone-free and supports full-swing input, which extends the dynamic range (DR). Overall, this work achieves 94.3dB DR with 40kHz BW and $67\mu\text{W}$ of power, leading to a DR FoM of 182dB.

Figure 9.3.1 shows the passive NS architecture. In the residue integration phase ϕ_{int} , the DAC C is connected to a capacitor $2C$, which realizes the passive integration of $0.2/(1-0.8z^{-1})$. In the conversion phase, ϕ_{conv} , $2C$ is split into 4 $C/2$ capacitors that are connected in series with C . This realizes the passive gain of 4 and the passive summation of V_{res} with $4V_{\text{int}}$. It reduces the comparator power by 25× compared to [1] with a multipath comparator, and by 2.8× compared to [2] with a passive gain of 2. In addition, its sharper NTF brings a 4.4dB SQNR benefit over [2]. By eliminating the residue sampling, the total kT/C noise is also reduced by 5.5×.

Figure 9.3.2 shows the ADC architecture with the 2nd-order MES technique. The DAC is segmented into 1 thermometer MSB and 2 binary LSB sections (LSB_1 and LSB_2). The MSB mismatch is addressed using DWA, while the LSB mismatch is addressed by the 2nd-order MES. 1st-order MES only needs to subtract the previous mismatch error $E(n-1)$, and thus, can be realized simply by delaying DAC reset [4]. By contrast, 2nd-order MES requires feeding back $2E(n-1)-E(n-2)$. To realize it, 2 identical $(1+2)$ LSB DACs are used, each of which alternatively produce $2E(n-1)$ and $E(n-2)$ via proper DAC control during sampling ϕ_s and reset ϕ_{rst} phases [5]. Feeding back previous LSB results causes ADC input range loss. Decreasing the LSB weight by increasing the MSB levels can minimize this loss, but cannot remove it (e.g., still 2dB loss with 9-level MSB [4]). To address this issue, this work uses digital prediction to feed opposite signals via the MSB DAC to cancel out the injected LSB signals [5]. As a result, it does not have any signal range loss, and its MSB DAC can be simplified to only 2 capacitors, each of which is 1/3 of the entire DAC array ($C=3 \times 2^{12}C_0$). During ϕ_{conv} , the MSB connections are determined via 3 comparisons $D_{M2:0}$ (see Fig. 9.3.8). A tri-level switching scheme is used to achieve an MSB quantization step of 2^{11} for $D_{M1:0}$ ($2 \times$ finer than the MSB capacitor weight of 2^{12}), so that the MSB quantization error can be covered by only 1 LSB section.

Figure 9.3.3 shows the operation of 2nd-order MES with digital prediction. For an odd ADC cycle $n=2k-1$, the bottom plates of LSB_1 and LSB_2 are connected to LSB codes $D_{L12:0}(2k-3)$ and $-D_{L12:0}(2k-2)$ during ϕ_s . Then, during ϕ_{rst} , the bottom plate of LSB_1 is reset to 0, while that of LSB_2 is reversed to $D_{L12:0}(2k-2)$. With these operations, mismatch errors $-E(2k-3)$ and $2E(2k-2)$ are injected to the sampled ADC input $V_{\text{in}}(2k-1)$. Then, in ϕ_{conv} , the SAR conversion is performed using MSB and LSB_1 , while LSB_2 remains unchanged. The LSB_1 switching produces a mismatch error $-E(2k-1)$. Thus, the total mismatch error incurred in cycle $2k-1$ is $E_{\text{tot}}(2k-1)=-E(2k-3)+2E(2k-2)-E(2k-1)$. In the next even cycle $n=2k$, the roles of LSB_1 and LSB_2 are flipped, leading to the total mismatch error of $E_{\text{tot}}(2k)=-E(2k-2)+2E(2k-1)-E(2k)$. Combining results of odd/even cycles, the overall mismatch error transfer function is $E_{\text{tot}}(z)=-(1-z^{-1})^2 \cdot E(z)$, which proves 2nd-order mismatch shaping [5].

As mentioned earlier, MES has a signal range loss issue. In the 2nd-order MES, since the conversion is performed using only 1 LSB DAC, the ADC conversion range is reduced to $\pm 5/6$ (MSB weight of 2/3 plus 1 LSB weight of 1/6). In addition, the total LSB feedback $2D_L(n-1)-D_L(n-2)$ takes up $\pm 1/2$ range (3 LSB weights of $3 \times 1/6$). Subtracting it out, the allowable ADC input range is only $\pm 1/3$, which is a 9.5dB DR loss. To address this issue, we estimate the total sampled signal $V_{\text{in}}(n)-2D_L(n-1)-D_L(n-2)$ by , perform a tri-level quantization to get $D_{P1:0}(n)$, and subtract it out by connecting it to MSB during ϕ_s . Since the MSB weight is 2/3, this recovers the full ADC input range of ± 1 .

Fabricated in 40nm CMOS, the prototype occupies 0.061mm^2 (Fig. 9.3.7) and consumes $67.4\mu\text{W}$ (DAC: $42\mu\text{W}$, comparator: $8.2\mu\text{W}$, bootstrap switches: $1.7\mu\text{W}$, digital: $15.5\mu\text{W}$) from 1.1V at 2MS/s. Figure 9.3.4 shows measured spectra with 1kHz input. Without MES and prediction (top left), the ADC has a maximum input range of -1.6dBFS ($\pm 5/6$). The spectrum shows 1st-order NS, but the DAC mismatch limits SNDR/SFDR. With 2nd-order MES and prediction enabled (bottom left), the input amplitude can reach the full swing of $2.2V_{\text{pp}}$. The SNDR/SFDR are improved to 90.5/102.2dB. The remaining tones are due to sampling nonlinearity. Figure 9.3.4 right compares spectra of 1st- and 2nd-order MES. Since this chip does not implement prediction for 1st-order MES, for fair comparison, prediction for 2nd-order MES is turned off. The input is lowered to -10dBFS to avoid saturation. The 2nd-order MES reduces the tones and noise floor. The advantage of the 2nd-order MES is more obvious with a smaller input (e.g., -44dBFS). Because 1st-order MES has a strong input dependence, it produces many tones, which do not exist in 2nd-order MES. Figure 9.3.5 shows an input amplitude sweep. Compared to 1st-order MES without prediction, 2nd-order MES with prediction improves DR by 11.3dB (3.8dB input range and 7.5dB SNDR improvements).

Figure 9.3.6 summarizes the performance and compares with other NS SAR ADCs. This work has a 2nd-order MES that supports full input range and aggressive mismatch shaping, and is tone-free at low signal amplitudes. The chip is PVT robust, calibration-free, and does not consume any static current. It realizes a passive gain of 4, which greatly reduces the comparator noise, and it does not add large kT/C noise. It is the first OTA-free NS-SAR ADC with $\text{ENOB} > 13\text{b}$.

Acknowledgements:

This work was supported by NSFC under Grant 61904094, Beijing National Research Center for Information Science and Technology, and Beijing Innovation Center for Future Chip.

References:

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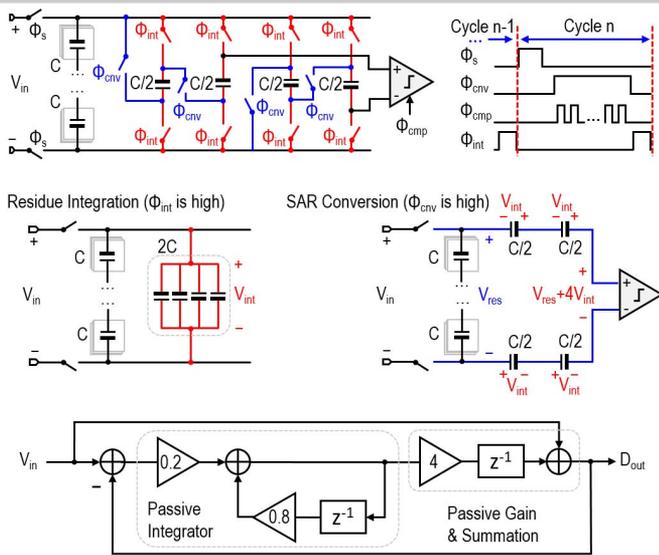


Figure 9.3.1: Principle of the proposed passive NS technique.

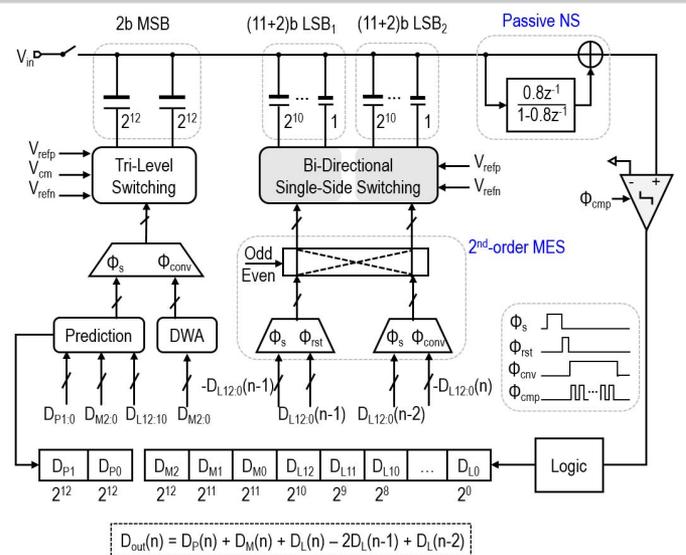


Figure 9.3.2: The proposed 13b NS SAR ADC with 2nd-order MES.

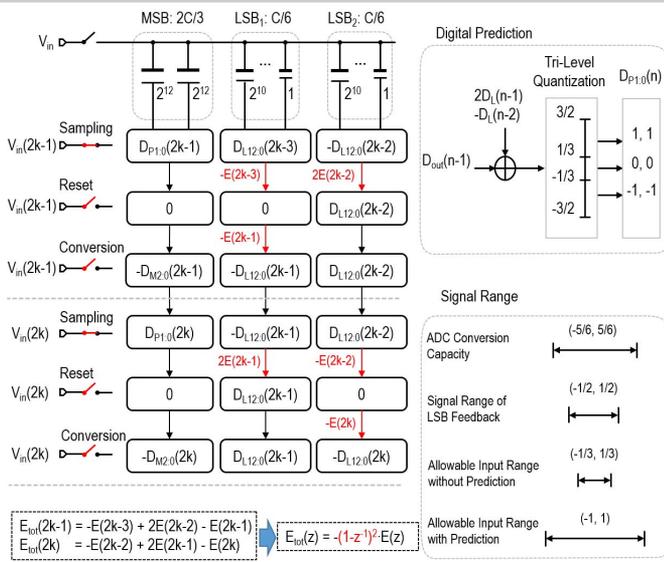


Figure 9.3.3: Illustration of the 2nd-order MES with digital prediction.

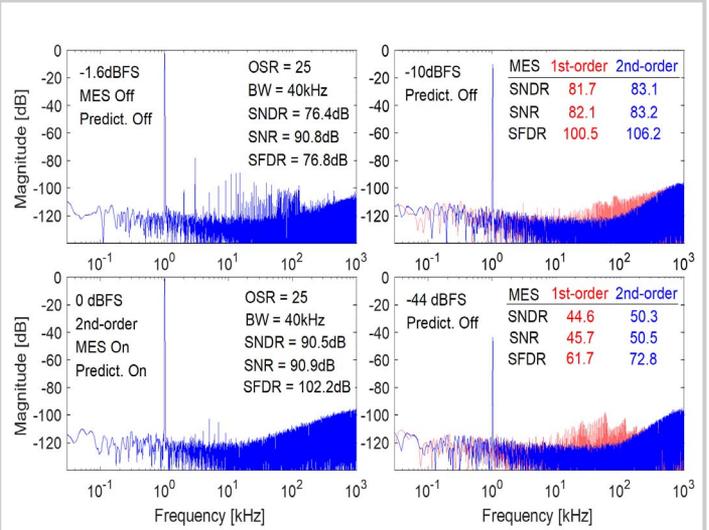


Figure 9.3.4: Measured output spectra under different conditions.

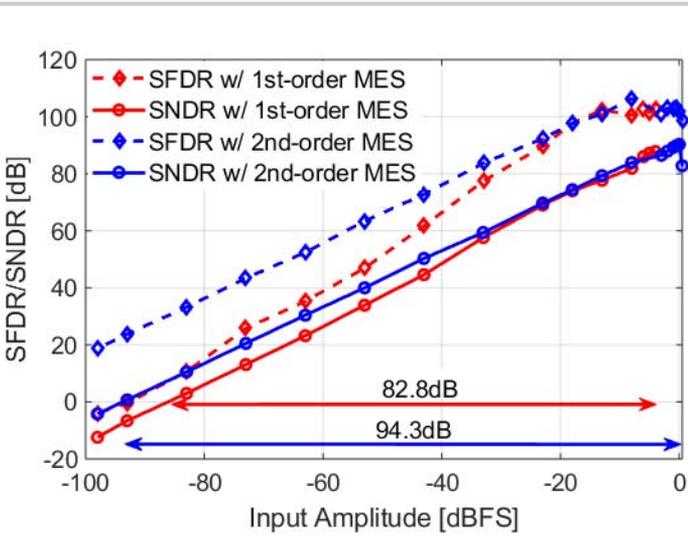


Figure 9.3.5: Measured SFDR/SNDR vs. input amplitudes.

	This work	ISSCC 16 Shu [4]	ISSCC 17 Liu [3]	ISSCC 18 Li	ISSCC 19 Lin [2]		
Process	40nm	55nm	28nm	40nm	14nm		
Architecture	Passive NS SAR	Active NS SAR	DA-based NS SAR	DA-based NS SAR	Passive NS SAR		
DAC Mismatch Solution	2 nd -order MES	1 st -order MES	DWA	FG Cal.	-		
OTA-Free	✓	×	✓	✓	✓		
PVT Robust	✓	✓	×	✓ (BG Cal.)	✓		
Supply (V)	1.1	1.2	1	1.1	0.9		
Area (mm ²)	0.061	0.072	0.0049	0.024	0.0021		
F _s (MS/s)	2	1	132	10	320		
Power (μW)	67.4	15.7	460	84	1250		
OSR	25	100	125	500	13.2	8	4
BW (kHz)	40	10	4	1	5000	625	40000
SFDR (dB)	102.2	102.2	105.1	105.1	92.6	89	77.4
SNR (dB)	90.9	96.1	96.8	104	80.1	-	67
SNDR (dB)	90.5	95.3	96.1	101	79.7	79	66.6
DR (dB)	94.3	98.5	-	101.7	81.8	80.5	-
FoM ₁ (dB)	178.2	177	180	178.9	180.1	178	171.7
FoM ₂ (dB)	182	180.2	-	179.6	182.2	179.5	-

Figure 9.3.6: Performance summary and comparison.

$$FoM_1 = SNDR + 10 \cdot \log_{10} \left(\frac{BW}{Power} \right), FoM_2 = DR + 10 \cdot \log_{10} \left(\frac{BW}{Power} \right)$$

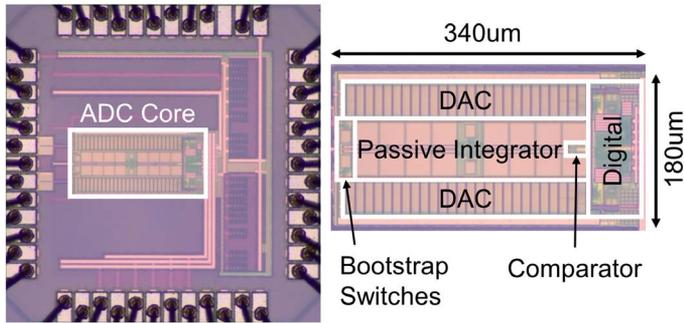


Figure 9.3.7: Die micrograph.

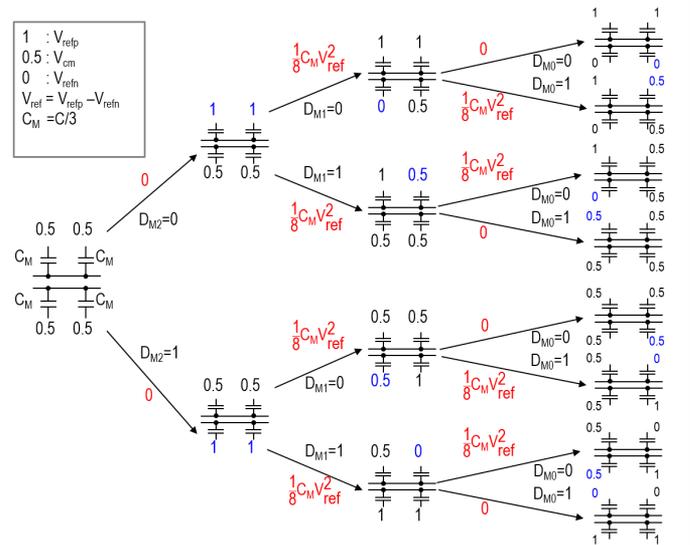


Figure 9.3.S1: The MSB switching scheme.