A 13-bit 0.005-mm^2 40-MS/s SAR ADC With kT/C Noise Cancellation

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***Abstract*— As any analog-to-digital converter (ADC) with a front-end sample-and-hold (S/H) circuit, successive approximation register (SAR) ADC suffers from a fundamental signal-to-noise ratio (SNR) challenge: its sampling kT/C noise. To satisfy the SNR requirement, the input capacitor size has to be sufficiently large, leading to a great burden for the design of the ADC input driver and reference buffer. This article presents an SAR ADC with a kT/C noise-cancellation technique. It enables the substantial reduction of ADC input capacitor size but without the large kT/C noise penalty. It greatly relaxes the requirement for ADC input driver and reference buffer. Built in 40-nm CMOS, a prototype 13-bit ADC has only 240-fF input capacitance and occupies a small area of 0.005 mm^2. Operating at 40 MS/s, it achieves a 69-dB signal-to-noise-and-distortion ratio (SNDR) across the Nyquist frequency band while consuming 591 μW of power.**

***Index Terms*— Amplifier noise, analog-to-digital converter (ADC), comparator preamp, input driver, kT/C noise cancellation, reference buffer, sampling noise, successive approximation register (SAR).**

I. Introduction

THE successive approximation register (SAR) is an attractive analog-to-digital converter (ADC) architecture in recent years. As shown in Fig. 1, an SAR ADC consists of a capacitor array, a comparator, and an SAR logic. The capacitor array, which serves as the sample-and-hold (S/H) circuit and also the digital-to-analog convertor (DAC), forms the input capacitor of an SAR ADC. Due to its simple structure and mostly digital implementation, the SAR ADC can achieve superior energy efficiency and is highly compatible with technology scaling. However, as any ADC with a front-end S/H circuit, SAR ADC suffers from a fundamental signal-to-noise ratio (SNR) challenge: its sampling kT/C noise. To satisfy the SNR requirement, the kT/C noise is typically suppressed by increasing the input capacitor size [1]–[12]. For example, the size of total differential input capacitors needs to be greater than 2.6 pF to achieve a kT/C noise-limited SNR of 80 dB with a 2.2-V peak-to-peak differential signal swing, and it has to be quadrupled for every 1-bit resolution increase. The large input capacitors make it very costly to design the ADC input driver and reference buffer. Their power, area, and design complexity are typically much higher than the SAR ADC itself.

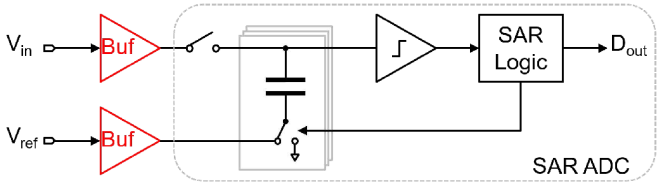

Fig. 1. SAR ADC with input driver and reference buffer.

To ease the ADC driver requirement, several researchers propose to embed a buffer inside the SAR ADC loop [13]–[15]. In this way, the S/H circuit is separated from the feedback DAC and shielded from the input by the buffer. The input capacitance of the ADC is only the input capacitance of the buffer and, thus, is substantially reduced, leading to a relaxed burden for the ADC input driver. Moreover, since the buffer resides inside the SAR loop, its nonlinear distortions during the sampling and conversion phases cancel with each other. Therefore, a simple source follower can be used as the buffer, reducing the design complexity. However, the source follower buffer still needs to drive large sampling capacitors limited by kT/C noise (e.g., 7 pF in [14]). It consumes extra power and can degrade the ADC power efficiency. In addition, these works [13]–[15] suffer from issues with their DACs. The current-steering DACs are used in [13] and [14] to feedback the conversion results, but they consume large static power. The work in [15] uses capacitive DACs to reduce power, but its large DAC size (2.9 times larger than the sampling capacitors) poses a great burden to the reference buffer.

Since the root cause of this problem is the large input capacitors, it is highly desirable to figure out ways to reduce the capacitor size but without incurring a large kT/C noise

Manuscript received March 30, 2020; revised June 22, 2020; accepted August 10, 2020. Date of publication August 25, 2020; date of current version November 24, 2020. This article was approved by Associate Editor John P. Keane. This work was supported in part by NSFC under Grant 61904094 and Grant 61934009, in part by the China Postdoctoral Science Foundation under Grant 2020M670329, in part by the Beijing National Research Center for Information Science and Technology, and in part by the Beijing Innovation Center for Future Chip. *(Corresponding author: Nan Sun.)*

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Digital Object Identifier 10.1109/JSSC.2020.3016656

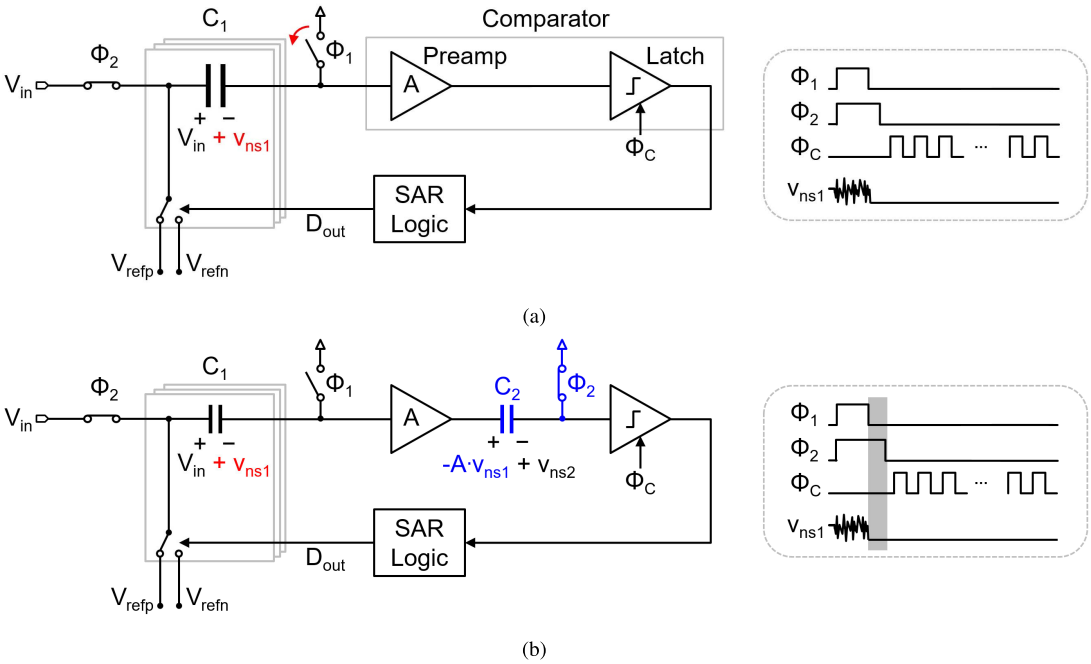


Fig. 2. (a) Conventional SAR ADC with bottom-plate sampling and comparator preamp. (b) Proposed SAR ADC with kT/C noise cancellation.

penalty. Recently, a two-step ADC with only 120-fF input capacitance is proposed [16]. It uses a continuous-time (CT) SAR as the first stage that is free from kT/C noise, as there is no sampling operation. Therefore, small input capacitors can be used. However, it suffers from several limitations. First, it cannot convert a dc signal since its input is ac coupled, limiting its applications. Second, the input signal frequency is limited to only 1 MHz to prevent large tracking errors from the CT SAR. Finally, the CT SAR operation has to be very fast. Each CT SAR cycle is only 500 ps. Even though the input capacitor size is reduced, ensuring settling within such a short time can still be a challenge for the ADC input driver and reference buffer.

This article presents an SAR ADC with a kT/C noise-cancellation technique. It enables the substantial reduction of input capacitor size but without the large kT/C noise penalty. Therefore, the requirements for both ADC input driver and reference buffer are relaxed. Compared with the SAR ADCs with loop-embedded buffers [13]–[15], the proposed technique eliminates the need for large internal sampling capacitors, reducing the power and area. Compared with the CT SAR work [16], this technique supports dc input and expands the signal bandwidth by 20 times. It also obviates the need for fast settling for the input driver and reference buffer. A prototype 13-bit SAR ADC is implemented in a 40-nm CMOS process to verify the proposed kT/C noise-cancellation technique. It has the total differential input capacitance of only 240 fF and occupies a small area of only 0.005 mm^2. Operating at 40-MS/s sampling rate and 1.1-V power supply, it achieves a 69-dB signal-to-noise-and-distortion ratio (SNDR) across the Nyquist frequency band while consuming 591 μW of power.

This article is an extension of [17]. It is organized as follows. Section II presents the operation principle of the SAR ADC with kT/C noise cancellation. Section III discusses several practical considerations in the ADC design. Section IV presents the circuit implementation. The measurement results are provided in Section V. Finally, Section VI concludes this article.

II. Proposed SAR ADC With kT/C Noise Cancellation

A. Basic Principle

Fig. 2(a) shows a conventional SAR ADC with bottom-plate sampling and a comparator preamp. This configuration is usually employed in high-resolution designs, where the bottom-plate sampling can improve sampling linearity and the preamp helps suppress the comparison noise. During the sampling phase, the input signal is tracked on the DAC, C_1, through two switches controlled by ϕ_1 and ϕ_2. When ϕ_1 falls, the charge on C_1 is trapped. Both the input signal, V_{in}, and the sampling noise, v_{ns1}, are frozen on C_1. The sampling noise directly adds to the input signal, leading to degraded SNR. The power of the sampling noise is

$$\overline{v_{\text{ns1}}^2} = \frac{kT}{C_1} \tag{1}$$

where k is Boltzmann's constant, and T is the absolute temperature [18]. To reduce v_{ns1} and, thus, improve SNR, the classic method is to use a large C_1, but this increases the burden for the ADC driver and reference buffer.

Examining the property of the sampling kT/C noise v_{ns1}, we can find that the time-varying noise voltage freezes to a constant voltage once the sampling switch ϕ_1 falls. It acts just like an offset voltage at the preamp input during the entire SAR conversion phase. This feature inspires us to treat it as an offset and manages to remove it through a cancellation technique that is based on the classic output series offset cancellation [19], [20]. This cancellation technique also shares

similarities with the correlated double-sampling (CDS) technique used in image sensors for mitigating the reset noise [21] as well as the noise-reducing enhancements in [22] and [23]. In [24], it is extended to implement a sampling circuit that is able to sample a time-varying signal while canceling the sampling noise.

Our proposed SAR ADC with kT/C noise cancellation is illustrated in Fig. 2(b). Compared with Fig. 2(a), the only additional circuits are a capacitor C_2 and a switch controlled by ϕ_2, placed between the comparator preamp and latch. For simplicity of explanation, let us consider a special case when V_{in} is a dc signal. In this case, after ϕ_1 falls, the voltage at the preamp input is fixed to be $-v_{\text{ns1}}$, exhibiting like an offset. As ϕ_2 falls later than ϕ_1, the "offset" $-v_{\text{ns1}}$ is amplified through the preamp and stored across C_2 during the time interval between the falling edges of ϕ_1 and ϕ_2. Since C_2 works in the output series offset-cancellation configuration, the kT/C_1 noise v_{ns1} is canceled at the right-hand side of C_2. When ϕ_2 falls, the kT/C_2 noise, v_{ns2}, is introduced. However, because it is after the preamp, its input referred noise is attenuated by the preamp gain A. In this way, the total sampling noise of proposed SAR ADC is only the attenuated kT/C_2 noise, as expressed follows:

$$\overline{v_{\text{ns}}^2} = \frac{\overline{v_{\text{ns2}}^2}}{A^2} = \frac{kT}{A^2 C_2}. \tag{2}$$

This result shows that kT/C_1 noise is canceled, and the kT/C_2 noise is attenuated. As a result, both C_1 and C_2 can be sized small but without incurring a large noise penalty.

B. Detailed Operation

The detailed operation of the proposed SAR ADC is shown in Fig. 3. An entire SAR operation cycle is divided into three phases: the C_1 sampling phase (from t_0 to t_1), the C_2 sampling phase (from t_1 to t_2), and the SAR conversion phase (from t_2 to the end).

When ϕ_1 is high, V_{in} is tracked on C_1. The preamp offset v_{os} is amplified and stored on C_2. When ϕ_1 falls, the C_1 sampling phase finishes, and C_1 stores both the sampled input signal and the kT/C_1 noise. The voltage across C_1 is frozen during the remaining time of the operation cycle, and it can be expressed as

$$V_{C_1} = V_{\text{in}}(t_1) + v_{\text{ns1}}. \tag{3}$$

When ϕ_1 falls, ϕ_2 is still high. Thus, the input signal sampling continues on C_2 after the preamp. The C_2 sampling finishes with the falling of ϕ_2. At this moment (t_2), the voltage at the preamp input is $V_{\text{in}}(t_2) - V_{\text{in}}(t_1) - v_{\text{ns1}} - v_{\text{os}}$. This voltage is amplified by A times and stored on C_2. When ϕ_2 falls, the kT/C_2 noise v_{ns2} is introduced on C_2. Thus, the total voltage frozen on C_2 after the falling of ϕ_2 is

$$V_{C_2} = A[V_{\text{in}}(t_2) - V_{\text{in}}(t_1) - v_{\text{ns1}} - v_{\text{os}}] + v_{\text{ns2}}. \tag{4}$$

After ϕ_2 falls, the SAR conversion phase starts. The digital codes are fed to the bottom plate of the DAC (i.e., the left-hand side of C_1), and the SAR logic attempts to bring the right-hand side of C_2 to zero. Ignoring other circuit non-idealities, the final digital output can be found to be

$$D_{\text{out}} = V_{\text{in}}(t_2) + v_{\text{ns2}}/A. \tag{5}$$

It shows that the kT/C_1 noise v_{ns1} is canceled and does not exist in D_{out}. Thus, theoretically speaking, C_1 can be made arbitrarily small but without incurring kT/C_1 noise penalty. The kT/C_2 noise v_{ns2} is suppressed, thus permitting the use of a small C_2. Note that the preamp offset V_{os} is also canceled. It means that the proposed kT/C noise-cancellation technique also lowers the ADC offset and the flicker noise. $V_{\text{in}}(t_1)$ does not show up in D_{out}. The final ADC output D_{out} corresponds to the input signal sampled at t_2, $V_{\text{in}}(t_2)$. This is because the real signal sampling is performed on C_2 at time t_2. The role of C_1 sampling is only to keep a small signal swing at the preamp input so that the preamp does not saturate during the C_2 sampling phase.

III. Practical Considerations

A. Incomplete kT/C_1 Noise Cancellation

For ease of explanation, we have so far assumed that the preamp fully settles during the C_2 sampling phase, thus leading to the complete noise cancellation. However, in a practical design, the preamp does not fully settle due to its finite bandwidth, as shown in Fig. 4 where the signal components are eliminated for simplification. The sampling kT/C_1 noise, v_{ns1}, can be considered as a small step signal presented at the preamp input. For a single-pole preamp with a settling time constant of τ, its response with respect to v_{ns1}, i.e., the noise voltage stored on C_2, can be expressed as

$$v_{\text{ns1},C2} = -A \cdot v_{\text{ns1}} \cdot (1 - e^{-\Delta t/\tau}) \tag{6}$$

where $\Delta t = t_2 - t_1$ is the duration of the C_2 sampling phase. When referring $v_{\text{ns1},C2}$ to the input, it cancels with v_{ns1}. Eventually, the input referred noise residue due to the incomplete cancellation can be obtained as

$$\overline{v_{\text{ns1,res}}^2} = \overline{v_{\text{ns1}}^2} \cdot e^{-2\Delta t/\tau} = kT/C_1 \cdot e^{-2\Delta t/\tau}. \tag{7}$$

To minimize the noise residue without increasing the input capacitor C_1, we face a tradeoff between Δt and τ. On one hand, the increase in Δt is limited by the signal swing of preamp [24], [25]. This is because the voltage change at the preamp input, $V_{\text{in}}(t_2) - V_{\text{in}}(t_1)$, is amplified during the C_2 sampling phase, as shown in Fig. 3. Thus, Δt needs to be made small to prevent the preamp from saturation and ensure sufficient linearity. On the other hand, reducing τ is at the expense of increased preamp power. In this design, $\Delta t/\tau$ is set to be 2 to achieve a reasonable tradeoff. According to (7), the residue noise is only 0.018 kT/C_1, which implies that more than 50 times kT/C_1 noise reduction is achieved.

B. Noise During C_2 Sampling Phase

During the C_2 sampling phase, the thermal noise is introduced across C_2. In Section II, the noise is simplified to be kT/C_2. For a complete analysis, we need to consider all the sources that contribute noise to C_2, including the switch at the

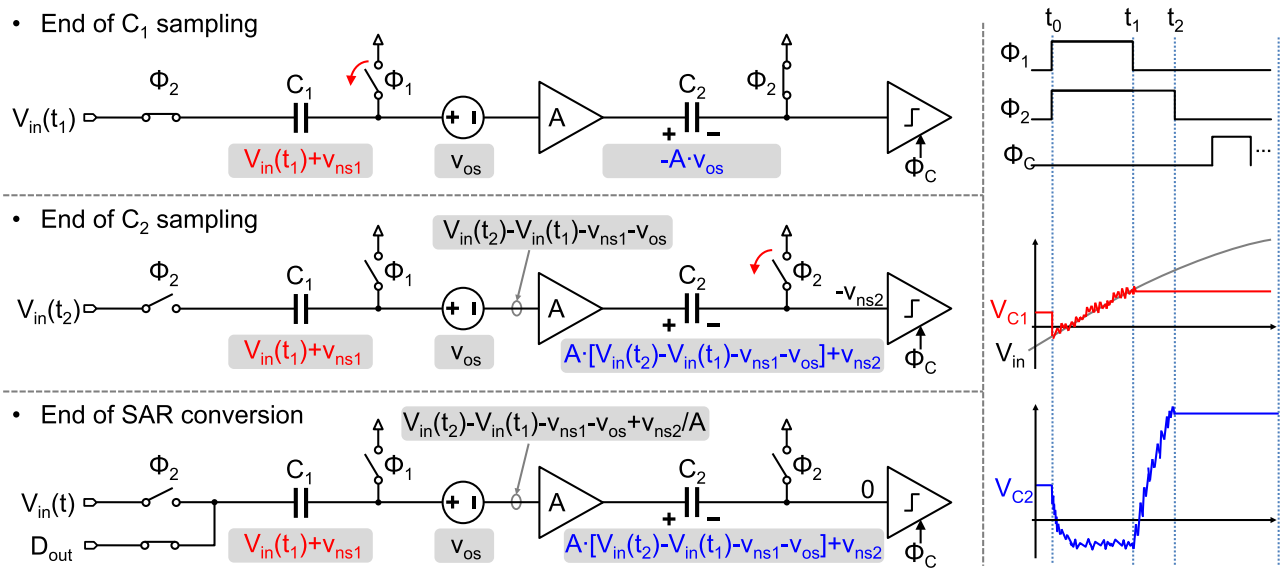


Fig. 3. Detailed operation scheme of the proposed SAR ADC.

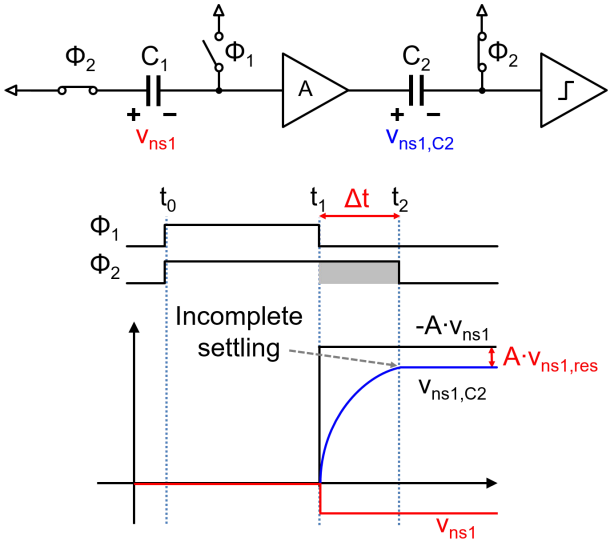


Fig. 4. Illustration of incomplete noise cancellation.

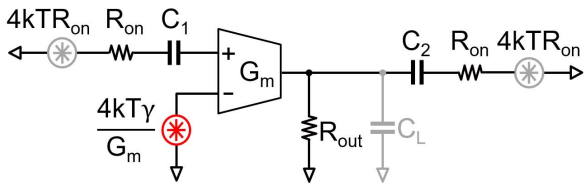


Fig. 5. Circuit model of noise during the C_2 sampling phase.

left-hand side of C_1, the switch at the right-hand side of C_2, and the preamp.

Fig. 5 provides the circuit model of noise during the C_2 sampling phase. In this figure, R_{ON} represents the ON-resistance of switch, G_m is the transconductance of preamp, and $R_{\mathrm{out}} = A/G_m$ is the output resistance of preamp. The single-end input referred noise power spectrum density (PSD) of a CMOS-input preamp used in this design is known to be

$$\frac{\overline{v_{\mathrm{nin,amp}}^2}}{\Delta f} = \frac{4kT\gamma}{G_m} \tag{8}$$

where γ is the device-dependent fitting parameter, and its theoretical value is 2/3 for long-channel devices [26].

For a power-efficient design, the circuit bandwidth is typically limited by the preamp rather than the switches. This necessitates the following relationship:

$$R_{\mathrm{ON}} \ll 1/G_m \ll R_{\mathrm{out}}. \tag{9}$$

Therefore, the preamp dominates the noise contribution during C_2 sampling phase. The noise bandwidth of the preamp (without C_L) during the C_2 sampling phase is about $1/4R_{\mathrm{out}}C_2$, leading to the input referred preamp noise of

$$\overline{v_{\mathrm{ns2},amp}^2} \simeq \frac{kT\gamma}{G_m R_{\mathrm{out}} C_2} = \frac{kT\gamma}{ac_2}. \tag{10}$$

It shows that this result is about A times larger than the foregoing simplified C_2 sampling noise in (2). By (10), there are two ways to reduce the preamp noise during C_2 sampling phase. One is to increase the preamp gain A, but a large A is undesired since it may cause saturation of the preamp. The other way is to increase C_2, but this increases the preamp settling time constant, leading to degraded kT/C_1 noise-cancellation effect.

In this design, we make careful considerations in dealing with the noise in this phase. First, the nominal value of the preamp gain is set to be $A = 6$ to provide effective noise suppression while keeping the preamp output swing within a reasonable range. It varies from $4\sim7$ across $1\sim1.2$-V supply, -40 °C$\sim$85 °C temperature range, and various process corners. Second, we add an additional load capacitor C_L at the preamp output to reduce the noise bandwidth. The reason that we do not directly increase C_2 is that C_L can also reduce the preamp noise during the SAR conversion phase, as will be discussed in detail later. With C_L, the input referred preamp noise during the C_2 sampling phase can be rewritten as

$$\overline{v_{\mathrm{ns2},amp}^2} \simeq \frac{kT\gamma}{A(C_2 + C_L)}. \tag{11}$$

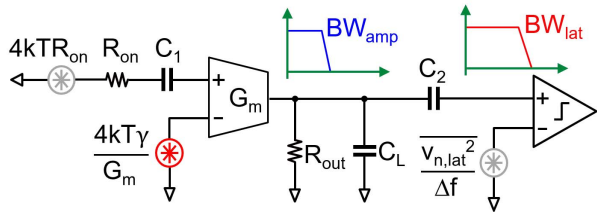


Fig. 6. Circuit model of noise during the SAR conversion phase.

Besides, in the practical design, the noise from the switch at the right-hand side of C_2 divides between C_2 and C_L. Therefore, the input referred switch noise across C_2 becomes

$$\overline{v_{\mathrm{ns2},kT/C2}^2} \simeq \frac{kTC_L}{A^2C_2(C_2+C_L)}. \tag{12}$$

C. Noise During SAR Conversion Phase

During the SAR conversion phase, there are also three noise sources: the DAC switch noise, the latch noise, and the preamp noise. The DAC switch noise is negligible compared with the preamp noise, as it has the same bandwidth as the preamp noise but a much smaller PSD. The noise from the latch is suppressed by the preamp gain and, thus, is also negligible. The dominant noise source in the SAR conversion phase is the noise from the preamp.

As shown in Fig. 6, the preamp noise is determined by two bandwidth limits. One is the bandwidth of the latch, $\mathrm{BW_{lat}}$, and the other is the bandwidth of the preamp itself, $\mathrm{BW_{amp}}$. As reducing $\mathrm{BW_{lat}}$ will lower the speed of the latch, we make $\mathrm{BW_{amp}}$ to be the bandwidth limit by setting a large load capacitor C_L. $\mathrm{BW_{lat}}$ is made much larger so that every comparison result can be resolved in half of a bit cycle under PVT variations. An issue of using $\mathrm{BW_{amp}}$ instead of $\mathrm{BW_{lat}}$ as the bandwidth limit is that the settling error during the SAR conversion phase is increased. This issue is addressed by adding redundant bits [27].

With this configuration, the preamp noise during the SAR conversion phase is obtained as

$$\overline{v_{\mathrm{nc,amp}}^2} = \frac{kT\gamma}{\mathrm{ac}_L}. \tag{13}$$

D. Noise Summary and Comparison

To evaluate the effect of the proposed kT/C noise-cancellation technique, Fig. 7 summarizes and compares the noise performance between two 13-bit SAR ADCs with and without kT/C noise cancellation. The preamp input capacitance C_p is also included to get accurate noise estimations. With $C_1 = 120$ fF, $C_2 = 50$ fF, $C_L = 100$ fF, $C_p = 20$ fF, and $A = 6$, the power of different noise sources can be obtained based on the abovementioned analysis. The input switch noise during C_2 sampling, DAC noise, and latch noise are small, and they are classified as others in Fig. 7.

It shows that the kT/C_1 noise accounts for 77% of the total noise in the conventional SAR without kT/C noise cancellation, while this percentage is reduced to be only 4% in the proposed SAR with kT/C noise cancellation. The preamp noise becomes the dominant noise source in the proposed SAR, which accounts for 59% of the total noise. Moreover, the proposed SAR has a larger amount of preamp noise than the conventional SAR since additional preamp noise is introduced during the C_2 sampling phase. Overall, 2.6 times total noise reduction is achieved by the proposed kT/C noise-cancellation technique.

It is worth noting that, except for the additional preamp noise during the C_2 sampling phase, another cost of the kT/C noise cancellation is that the preamp in the proposed SAR consumes more power than that in the conventional SAR. This is because the preamp needs to settle rapidly during the C_2 sampling phase. To get a general idea, Fig. 8 provides a timing diagram to illustrate the additional preamp power qualitatively. In this design, all the controlling signals, including ϕ_1, ϕ_2, and ϕ_c, are generated from a master clock ϕ_m. The time duration of the C_2 sampling phase (Δt) is set by using half of the master clock cycle, keeping the signal swing at the preamp input within a reasonably small range during this phase. Every bit decision takes an entire master clock cycle (the time duration is $2\Delta t$), in which half of a master clock is used for the latch regeneration (t_{lat}) and the other half is occupied by logic delay (t_d), DAC settling (t_{DAC}), and preamp settling (t_{amp}). As t_d and t_{DAC} are much smaller than t_{amp}, we can approximately consider $t_{\mathrm{amp}} \approx \Delta t$. For the conventional SAR, the preamp settling requirement is determined by the settling during the conversion phase. The preamp load capacitor in this phase is $C_L = 100$ fF, while, for the proposed SAR, the preamp settling requirement is determined by the settling in the C_2 sampling phase, and the preamp load capacitor is $C_L + C_2 = 150$ fF. Assuming the same settling in the two cases (e.g., $\Delta t = 2\tau$ to achieve 86% voltage settling), the preamp in the proposed SAR needs to consume 50% more power than that in the conventional SAR.

It is meaningful to compare the overhead of this work with that of SAR ADCs without kT/C noise cancellation. In order to achieve the same input-referred noise as the proposed work, the conventional SAR in Fig. 7 has to increase its input capacitance C_1 to at least 800 fF, which is 6.7 times larger than that of the proposed work. As has been revealed in many studies [28]–[31], the power of ADC input driver and reference buffer is typically much larger than that of the ADC core. Because of the power of driver and buffer scales with the ADC input capacitance, the additional preamp power in the proposed work is worthwhile when considering the significantly reduced cost on the input driver and reference buffer enabled by using small input capacitors.

E. Other Non-Idealities of Preamp

In this section, we discuss other non-idealities of the preamp, including the preamp input capacitance, the preamp delay, and the gain nonlinearity.

The preamp input capacitance has two consequences. First, it attenuates the signal at preamp input, leading to increased total ADC input-referred noise. In this design, with 20-fF preamp input capacitance and 120-fF ADC input capacitance, the SNR loss is 1.3 dB. Second, the nonlinear capacitance at preamp input can cause nonlinear distortions. However, with 20-MHz input bandwidth, 1.1-V input amplitude, and

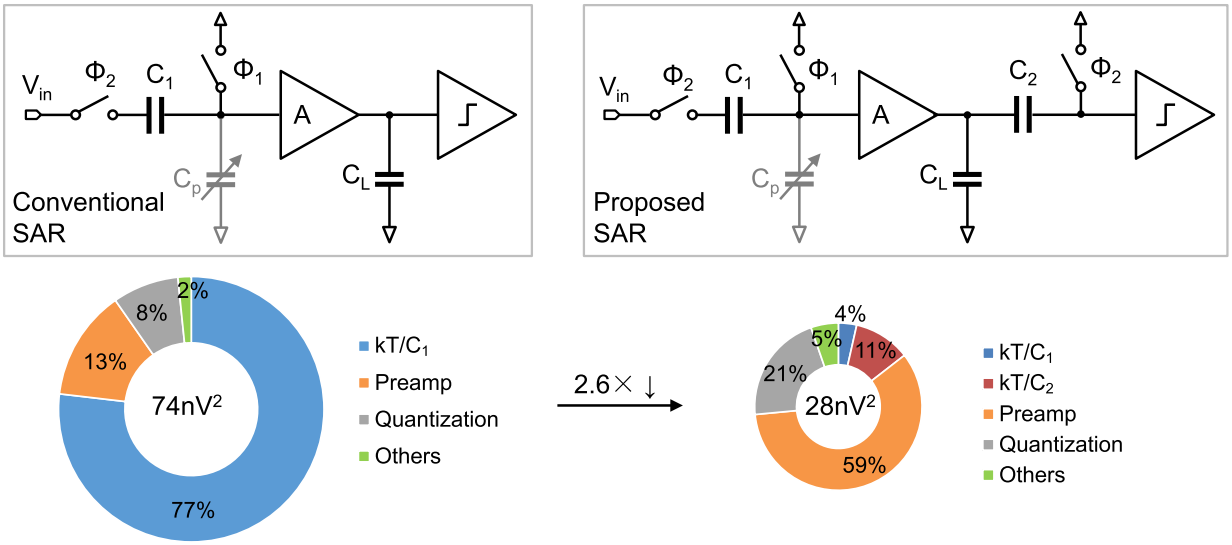


Fig. 7. Noise summary and comparison between SAR ADCs with and without kT/C noise cancellation.

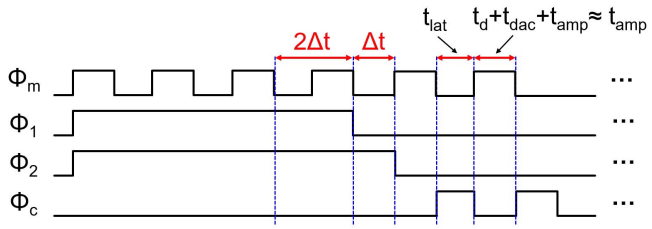


Fig. 8. Timing diagram for illustrating the cost on preamp power.

$\Delta t = 0.6$ ns in this design, the maximum signal swing at the preamp input is only 80 mV. Such a small signal swing introduces negligible nonlinear distortions.

Our previous analysis in Fig. 3 assumes that the input variation during the C_2 sampling phase is instantly amplified by the preamp and stored in C_2 as $A[V_{\text{in}}(t_2) - V_{\text{in}}(t_1)]$. In reality, the preamp experiences a delay when it transfers the high-frequency input variation from its input to output. Therefore, only a part of the amplified input variation is stored in C_2. The operation of the proposed SAR ADC with the preamp delay is illustrated in Fig. 9(a), where the noise components are not shown for simplification as we only discuss the issues with the input signal here. The preamp output during the C_2 sampling phase is analyzed in the Appendix. It shows that the preamp delay t_d is approximately equal to the preamp settling time constant τ across the Nyquist band. As with that in any input driver and buffer, t_d does not introduce distortion. With t_d, the voltage at the preamp output at the end of the C_2 sampling phase (i.e., voltage frozen on C_2) becomes

$$V_{C2}(t_2) \approx A[V_{\text{in}}(t_2 - t_d) - V_{\text{in}}(t_1)]. \tag{14}$$

Without considering other circuit non-idealities, the voltage at preamp output goes back to $V_{C2}(t_2)$ at the end of the SAR conversion. Since the voltage at preamp input settles to dc during the conversion phase, it is fully amplified and can be derived to be $V_{\text{in}}(t_2 - t_d) - V_{\text{in}}(t_1)$ when the SAR conversion finishes. Therefore, the final digital output is obtained as

$$D_{\text{out}} = V_{\text{in}}(t_2 - t_d). \tag{15}$$

Since the preamp is involved in the input sampling in the proposed SAR ADC, its gain nonlinearity needs to be paid attention. As indicated in (15), the gain nonlinearity can be canceled in the SAR loop and do not show up in the digital output, as long as the preamp gain at the end of the C_2 sampling phase matches that of the SAR conversion phase. However, the complete nonlinearity cancellation is only valid with infinite preamp bandwidth. Note that the signal at preamp input during the C_2 sampling phase is high-frequency (dc$\sim$20 MHz), but it settles to dc at the end of SAR conversion phase. The frequency difference between the two phases would cause the gain mismatch for a preamp with finite bandwidth. As shown in Fig. 9(b), if the gains of the two phases do not match, the final digital output becomes

$$D_{\text{out}} = \frac{A}{A'} V_{\text{in}}(t_2 - t_d) - \frac{A - A'}{A'} V_{\text{in}}(t_1) \tag{16}$$

where A' is the gain at the end of SAR conversion. In this case, a part of the nonlinearities in A and A' would leak to the digital output. Nevertheless, we can expect a good match between A and A' in general. The reasons are twofold. First, the preamp bandwidth (525 MHz) is much larger than the input signal bandwidth (20 MHz), leading to nearly constant preamp gain across the signal band. Second, the preamp operation conditions are similar at the ends of the two phases. The preamp output voltages are the same, and its input voltages are small and close. Therefore, the bulk of preamp nonlinearities can be suppressed. In a practical design, when high linearity is required, we can increase the preamp bandwidth to further minimize the gain variation across the signal band or reduce the time duration of the C_2 sampling phase to lower the signal swings at preamp input and output. Both approaches help improve the gain matching and linearity. However, they come with the cost too: the former directly increases the preamp power, and the latter can degrade the kT/C noise-cancellation effect.

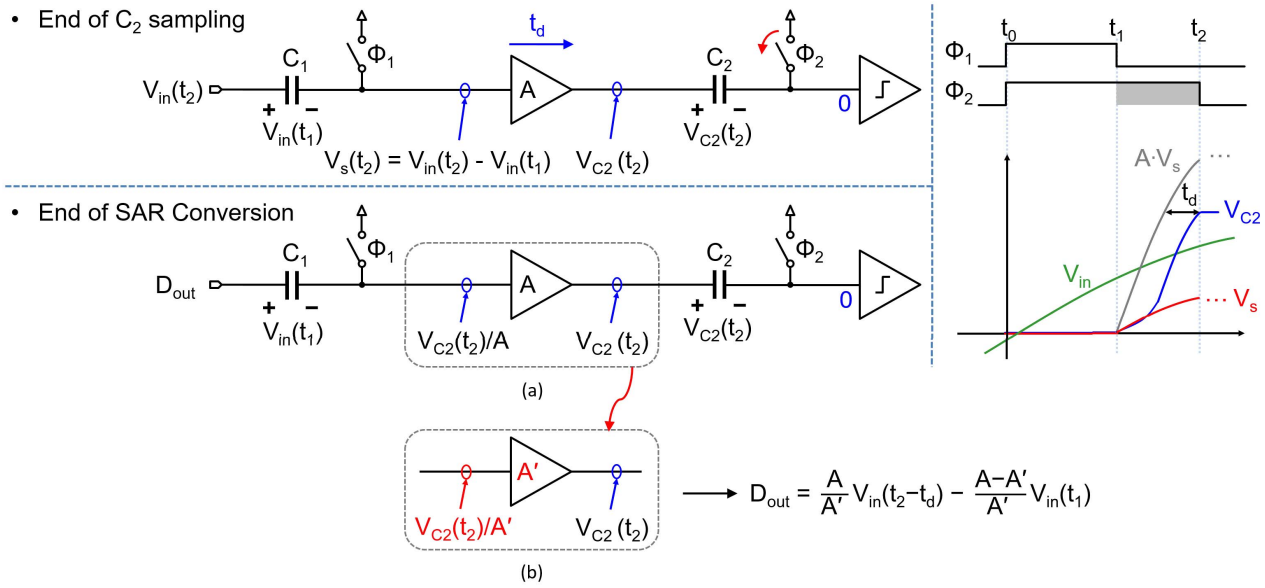


Fig. 9. Operation of the proposed SAR ADC with (a) preamp delay and (b) preamp gain mismatch.

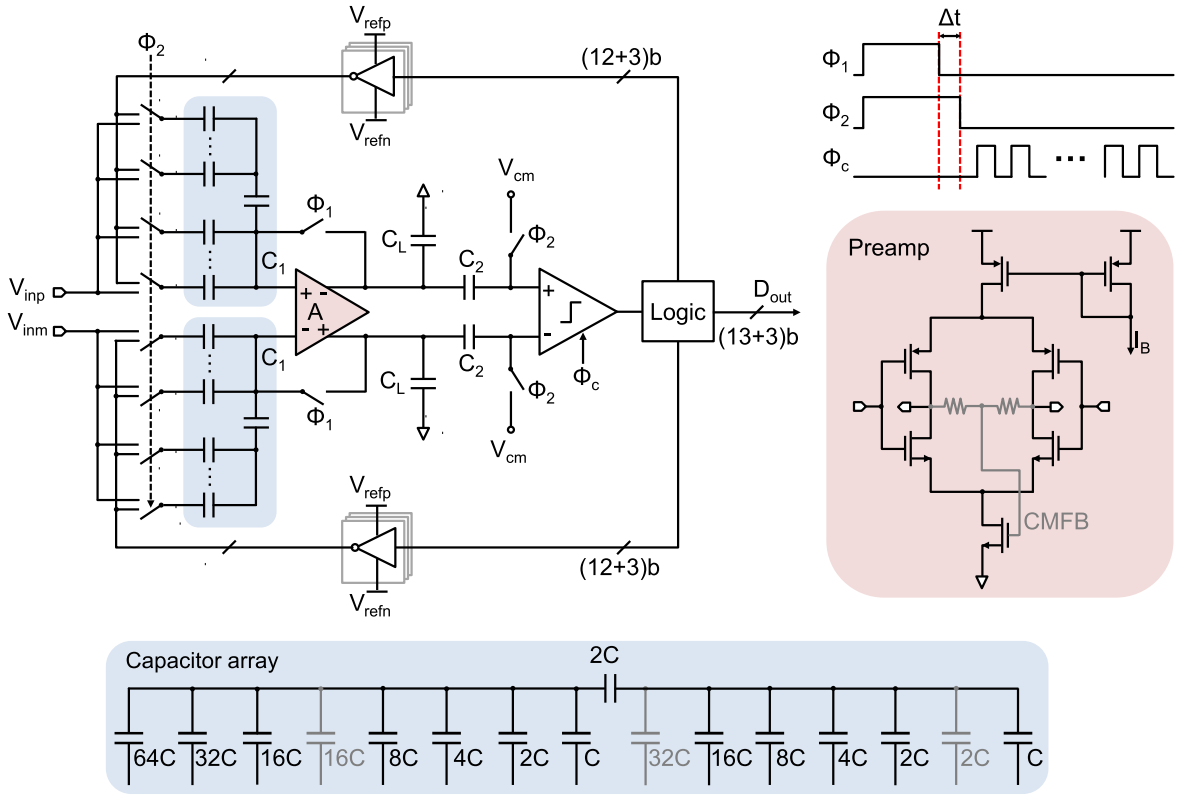


Fig. 10. Circuit implementation.

IV. Circuit Implementation

Fig. 10 shows the circuit implementation of the proposed SAR ADC. It adopts a differential structure to reject the common-mode (CM) circuit errors, including the charge injection from switches and the kick-back noise from the latch. The overall circuit is compact, and the hardware overhead is low. A slight difference from the single-end architecture in Fig. 2(b) is that the ϕ_1 switch connects the preamp input not to an ac ground, but to the preamp output. This way, a large portion of the preamp offset is canceled directly at the preamp input, which helps lower the preamp output signal swing. The synchronous SAR logic is used. The master clock frequency is 800 MHz, and the ADC sampling rate is 40 MS/s. The C_2 sampling phase is about 0.6 ns, which is set by using half of the master clock cycle.

Since the single-end input capacitor C_1 is only 120 fF, it adopts a bridge capacitor array topology to keep a reasonable unit capacitor size of 0.85 fF. Three redundant capacitors are

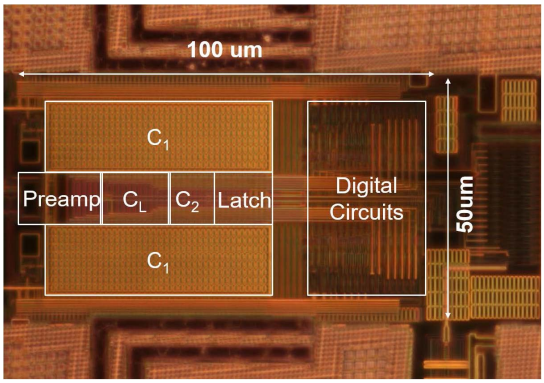
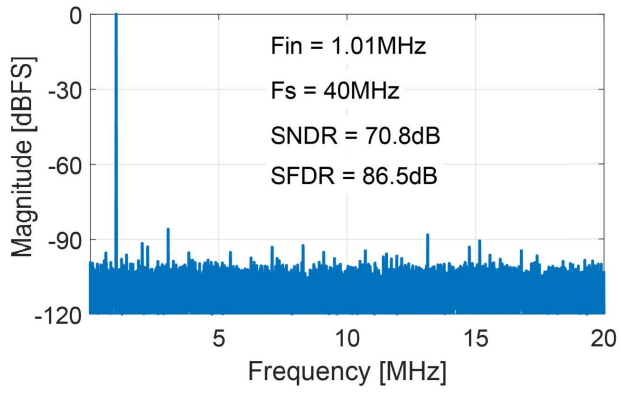
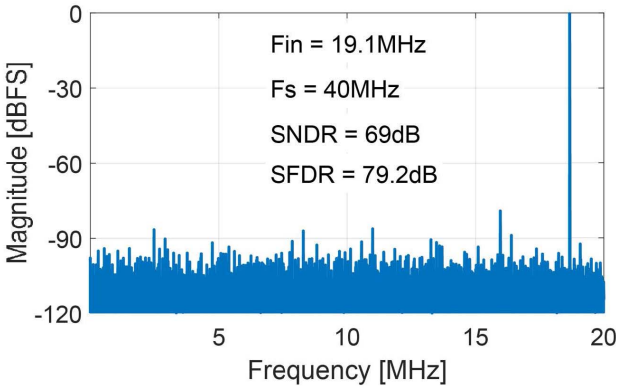


Fig. 11. Die photograph.



(a)

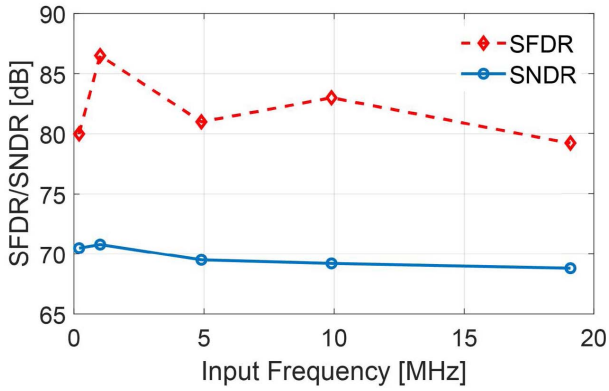


(b)

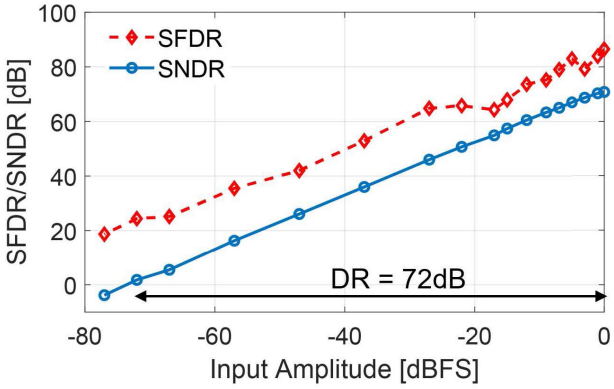
Fig. 12. Measured ADC output spectra with (a) 1.01-MHz input and (b) 19.1-MHz input.

added to tolerate the intermediate conversion errors. A foreground calibration is applied to address the capacitor mismatch issue [32].

The comparator preamp is a single-stage common-source amplifier. It adopts a CMOS input stage to double the current efficiency. A resistor divider is used to sense the output CM voltage and bias the tail NMOS transistor; this realizes the CM feedback (CMFB) circuit. Based on post-layout simulations, the preamp achieves the dc gain of 6 and the −3-dB bandwidth of 525 MHz while consuming 280-μW power from a 1.1-V supply. The comparator latch used in this design is a classic StrongARM latch [33].



(a)



(b)

Fig. 13. Measured SNDR/SFDR versus (a) input frequency and (b) input amplitude.

V. Measurement Results

This prototype SAR ADC is fabricated in a 40-nm CMOS process. The die photograph is shown in Fig. 11. Due to the significantly reduced capacitor size, the active area of the proposed SAR ADC is only 0.005 mm^2. At the sampling rate of 40 MS/s, the total power consumption is 591 μW with a 1.1-V power supply. The power breakdown is 28 μW for the DAC, 280 μW for the comparator preamp, 75 μW for the comparator latch and other analog circuits, and 208 μW for the digital circuits.

Fig. 12(a) and (b) shows the measured spectra with the full swing input signals of 2.2-V peak-to-peak differential voltage. With input at 1.01 MHz, the measured SNDR and spurious-free dynamic range (SFDR) are 70.8 and 86.5 dB, respectively. With input at 19.1 MHz, the measured SNDR and SFDR are 69 and 79.2 dB, respectively.

Fig. 13(a) and (b) provides the measured performance versus input frequency and input amplitude. It shows that the SNDR and SFDR are above 69 and 79.2 dB across the entire Nyquist band, respectively. The measured dynamic range (DR) with 1.01-MHz input frequency is 72 dB; this translates to the input-referred noise voltage of 194 μV_{rms}.

The performance of this work is summarized and compared with prior works in Table I. Compared with the prior kT/C noise reduction work [16], this work supports dc input and

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART ADCS

	This work	ISSCC 19' [16]	ISSCC 15' [14]	JSSC 20' [6]	JSSC 20' [7]	JSSC 17' [8]	JSSC 17' [9]	JSSC 15' [10]	ISSCC 15' [11]	ISSCC 13' [12]
Technology	**40 nm**	40 nm	40 nm	40 nm	40 nm	40 nm	65 nm	90 nm	65n m	65 nm
Architecture	**SAR**	CT SAR	SAR	SAR	SAR	SAR	SAR	SAR	Pipe-SAR	SAR
Resolution (bits)	**13**	13	14	14	10	15	12	13	13	14
ADC Input Cap. (pF)	**0.24**	0.12	0.4	8.2	2.1	16	18	4	4	8.2
Internal Sampling Cap. (pF)	**0.3**	0.3	7	-	-	-	-	-	0.67	-
kT/C Noise Suppressed?	√	√	×	×	×	×	×	×	×	×
Applicable for DC/HF Signal?	√	×	√	√	√	√	√	√	√	√
Area (mm^2)	**0.005**	0.01	0.236	0.08	0.023	0.32	0.105	0.097	0.054	0.55
Sampling Rate (MS/s)	**40**	2	35	4	120	0.02	0.04	50	50	80
$SFDR_{NYQ}$ (dB)	**79.2**	79.4	90	98	71.7	95.1	88.2	85	84.6	80.3
$SNDR_{NYQ}$ (dB)	**69**	71.7	74.4	75.4	54.9	74.1	64.2	71	70.9	71.3
Power (uW)	**591**	25	42500	157	1120	1.17	0.375	4200	1000	31100
FoMs (dB)	**174.3**	177.8	160.6	176.5	162	173.4	171.5	168.7	174.9	164.7
FoMw (fJ/conv-step)	**6.4**	3.9	283	9.6	20.5	14.1	7.1	29	6.9	129

expands the signal bandwidth by 20 times. It also obviates the need for fast settling for the ADC input driver and reference buffer. Compared with the SAR ADC with loop-embedded buffer [14], this work reduces the internal sampling capacitor size by 23 times because its kT/C noise is greatly suppressed. Compared with other state-of-the-art ADC works without kT/C noise reduction [6]–[12], it significantly reduces the input capacitor size. Hence, it can greatly relax the requirement on the ADC input driver and reference buffer, leading to significant power savings on the system level. In addition, due to the substantial reduction in the capacitor size, this chip has the smallest reported area among all published state-of-the-art Nyquist ADCs with ≥11-bit ENOB [34].

VI. CONCLUSION

This work proposes an SAR ADC with a kT/C noise-cancellation technique. It has a compact structure and requires little additional circuits over a conventional SAR ADC. It reduces the front-end sampling kT/C noise by more than 50 times and, thereby, permits the use of small input capacitance of only 240 fF for a 13-bit ADC. Due to the substantially reduced input capacitor size, the design requirement for ADC input driver and reference buffer is eased, leading to significant power and area savings at the system level.

In this prototype SAR ADC, the further signal bandwidth and noise suppression improvements are limited by the preamp bandwidth. Nevertheless, this technique is applicable to other ADC architectures for expanding the performance. It can be easily adopted in a pipeline or time-interleaved structure to boost the operation speed. It can also be used to achieve high resolution in oversampling ADCs where the preamp bandwidth requirement is relaxed.

APPENDIX
ANALYSIS ON PREAMP OUTPUT DURING C_2 SAMPLING

For the single-stage preamp, its transfer function can be expressed as

$$A(s) = \frac{A}{1 + s\tau}. \tag{17}$$

As shown in Fig. 9(a), the signal at the preamp input during the C_2 sampling phase (from t_1 to t_2) can be expressed as

$$V_s(t) = \begin{cases} 0, & \text{for } t = t_1 \\ V_{\text{in}}(t) - V_{\text{in}}(t_1), & \text{for } t_1 < t \le t_2. \end{cases} \tag{18}$$

The initial state at preamp output, i.e., the voltage stored on C_2 at t_1, is $V_{C2}(t_1) = 0$.

With these conditions, the complete response of the preamp output at the end of the C_2 sampling phase can be obtained as

$$V_{C2}(t_2) = [A_0 V_{\text{in}}(t_2 - t_d) - \text{AV}_{\text{in}}(t_1)] + [A V_{\text{in}}(t_1) - A_0 V_{\text{in}}(t_1 - t_d)] e^{-(t_2 - t_1)/\tau} \tag{19}$$

where $A_0 = A/(1 + (2\pi f \tau)^2)^{1/2}$, f is the input signal frequency, and t_d is the preamp delay and can be expressed as

$$t_d = \frac{\arctan(2\pi f \tau)}{2\pi f}. \tag{20}$$

Examining (19), it can be found that all the components of $V_{C2}(t_2)$ are linear. Since the preamp bandwidth (∼525 MHz) is much larger than the input signal bandwidth (≤20 MHz), i.e., $2\pi f \tau \approx 0$, we can get $t_d \approx \tau$ and $A_0 \approx A$. Besides, the second term in (19) is within 5 mV with $(t_2 - t_1)/\tau = 2$ in this design. It is much smaller than the first term that has a

swing of about 500 mV and, thus, can be neglected to simplify the expression of $V_{C2}(t_2)$. In this way, $V_{C2}(t_2)$ is rewritten as

$$V_{C2}(t_2) = A[V_{\text{in}}(t_2 - t_d) - V_{\text{in}}(t_1)]. \quad (21)$$

REFERENCES

[1] Y.-S. Shu and B.-S. Song, "A 15-bit linear 20-MS/s pipelined ADC digitally calibrated with signal-dependent dithering," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 342–350, Feb. 2008.

[2] P. Harpe, E. Cantatore, and A. van Roermund, "An oversampled 12/14b SAR ADC with noise reduction and linearity enhancements achieving up to 79.1dB SNDR," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Feb. 2014, pp. 194–195.

[3] B. Verbruggen, K. Deguchi, B. Malki, and J. Craninckx, "A 70 dB SNDR 200 MS/s 2.3 mW dynamic pipelined SAR ADC in 28nm digital CMOS," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2014, pp. 1–2.

[4] C.-H. Chan *et al.*, "60-dB SNDR 100-MS/s SAR ADCs with threshold reconfigurable reference error calibration," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2576–2588, Oct. 2017.

[5] H. Huang, H. Xu, B. Elies, and Y. Chiu, "A non-interleaved 12-b 330-MS/s pipelined-SAR ADC with PVT-stabilized dynamic amplifier achieving sub-1-dB SNDR variation," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3235–3247, Dec. 2017.

[6] Z. Zhu, X. Zhou, Y. Du, Y. Feng, and Q. Li, "A 14-bit 4-MS/s VCO-based SAR ADC with deep metastability facilitated mismatch calibration," *IEEE J. Solid-State Circuits*, vol. 55, no. 6, pp. 1565–1576, Jun. 2020.

[7] Y. Shen *et al.*, "A 10-bit 120-MS/s SAR ADC with reference ripple cancellation technique," *IEEE J. Solid-State Circuits*, vol. 55, no. 3, pp. 680–692, Mar. 2020.

[8] M. Shim *et al.*, "Edge-pursuit comparator: An energy-scalable oscillator collapse-based comparator with application in a 74.1 dB SNDR and 20 kS/s 15 b SAR ADC," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1077–1090, Apr. 2017.

[9] M. Liu, A. H. M. van Roermund, and P. Harpe, "A 7.1-fJ/conversion-step 88-dB SFDR SAR ADC with energy-free 'Swap to Reset,'" *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2979–2990, Nov. 2017.

[10] T. Miki *et al.*, "A 4.2 mW 50 MS/s 13 bit CMOS SAR ADC with SNR and SFDR enhancement techniques," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1372–1381, Jun. 2015.

[11] Y. Lim and M. P. Flynn, "A 1 mW 71.5 dB SNDR 50 MS/s 13 bit fully differential ring amplifier based SAR-assisted pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2901–2911, Dec. 2015.

[12] R. Kapusta, J. Shen, S. Decker, H. Li, E. Ibaragi, and H. Zhu, "A 14b 80 MS/s SAR ADC with 73.6 dB SNDR in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3059–3066, Dec. 2013.

[13] K. Doris, E. Janssen, C. Nani, A. Zanikopoulos, and G. van der Weide, "A 480 mW 2.6 GS/s 10b time-interleaved ADC with 48.5 dB SNDR up to nyquist in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2821–2833, Dec. 2011.

[14] M. J. Kramer, E. Janssen, K. Doris, and B. Murmann, "A 14 b 35 MS/s SAR ADC achieving 75 dB SNDR and 99 dB SFDR with loop-embedded input buffer in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2891–2900, Dec. 2015.

[15] T. Kim and Y. Chae, "A 2MHz BW buffer-embedded noise-shaping SAR ADC achieving 73.8dB SNDR and 87.3dB SFDR," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2019, pp. 1–4.

[16] L. Shen *et al.*, "A two-step ADC with a continuous-time SAR-based first stage," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3375–3385, Dec. 2019.

[17] J. Liu, X. Tang, W. Zhao, L. Shen, and N. Sun, "A 13b 0.005 mm^2 40MS/s SAR ADC with kT/C noise cancellation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 258–259.

[18] J. Pierce, "Physical sources of noise," *Proc. IRE*, vol. 44, no. 5, pp. 601–608, May 1956.

[19] R. Poujois, B. Baylac, D. Barbier, and J. Ittel, "Low-level MOS transistor amplifier using storage techniques," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 16, Feb. 1973, pp. 152–153.

[20] B. Razavi and B. A. Wooley, "Design techniques for high-speed, high-resolution comparators," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1916–1926, Dec. 1992.

[21] M. H. White, D. R. Lampe, F. C. Blaha, and I. A. Mack, "Characterization of surface channel CCD image arrays at low light levels," *IEEE J. Solid-State Circuits*, vol. JSSC-9, no. 1, pp. 1–12, Feb. 1974.

[22] T. Sugiki *et al.*, "A 60 mW 10 b CMOS image sensor with column-to-column FPN reduction," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2000, pp. 108–109.

[23] S. Yoshihara *et al.*, "A 1/1.8-inch 6.4 MPixel 60 frames/s CMOS image sensor with seamless mode change," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2998–3006, Dec. 2006.

[24] R. Kapusta, H. Zhu, and C. Lyden, "Sampling circuits that break the kT/C thermal noise limit," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1694–1701, Aug. 2014.

[25] R. Kapusta, H. Zhu, and C. Lyden, "Sampling circuits that break the kT/C thermal noise limit," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2013, pp. 57–60.

[26] A. A. Abidi, "High-frequency noise measurements on FET's with small dimensions," *IEEE Trans. Electron Devices*, vol. 33, no. 11, pp. 1801–1805, Nov. 1986.

[27] C.-C. Liu *et al.*, "A 10b 100MS/s 1.13 mW SAR ADC with binary-scaled error compensation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2010, pp. 386–387.

[28] C.-C. Liu, M.-C. Huang, and Y.-H. Tu, "A 12 bit 100 MS/s SAR-assisted digital-slope ADC," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2941–2950, Dec. 2016.

[29] W.-H. Tseng, W.-L. Lee, C.-Y. Huang, and P.-C. Chiu, "A 12-bit 104 MS/s SAR ADC in 28 nm CMOS for digitally-assisted wireless transmitters," *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2222–2231, Oct. 2016.

[30] H. S. Bindra, J. Lechevallier, A.-J. Annema, S. Louwsma, E. van Tuijl, and B. Nauta, "Range pre-selection sampling technique to reduce input drive energy for SAR ADCs," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2017, pp. 217–220.

[31] H. S. Bindra, A.-J. Annema, G. Wienk, B. Nauta, and S. M. Louwsma, "A 4MS/s 10b SAR ADC with integrated class—A buffers in 65nm CMOS with near rail-to-rail input using a single 1.2 V supply," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2019, pp. 1–4.

[32] S.-W. M. Chen and R. W. Brodersen, "A 6-bit 600-MS/s 5.3-mW Asynchronous ADC in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2669–2680, Nov. 2006.

[33] J. Montanaro *et al.*, "A 160-MHz, 32-b, 0.5-W CMOS RISC microprocessor," *IEEE J. Solid-State Circuits*, vol. 31, no. 11, pp. 1703–1714, Nov. 1996.

[34] B. Murmann. *ADC Performance Survey 1997–2020*. Accessed: Aug. 10, 2020. [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html

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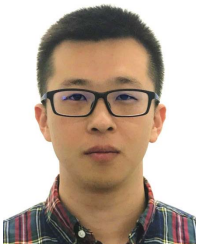

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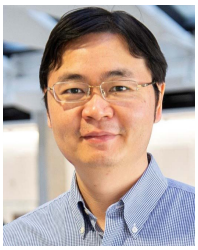

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